TriJmos – Triode and jFET model using the VDMOS

An Appendix to PAK213 – Triode Tube modelling

 ver 1v0 13 Feb 2023

for models https://PAKlaunchSite.jimdo.com/Spice-Models/

The VDMOS model as used in the LTspice simulator can model power MOSFETs nicely. Mike Engelhardt kindly updated the VDMOS (May 2019) to include temperature parameters. My earlier Triode+jFET subcircuit has been updated with the new VDMOS temperature parameters.

My updated model is called the TriJmos model because it models triodes, SITs and jFETs. This paper explains the TriJmos model with 17 examples.

The updated TriJmos subcircuit includes:

- jFET gate-drain leakage current (I_{GSX}) changing with Vds and temperature
- Quasi-saturation [footnote [1]] is significant for most small-signal jFETs
- Noise parameters are included
- Triode Island effect is accurately and easily fitted using table parameters
- Triode grid current includes modulation by anode voltage

All these effects are built into 1 *generic* subcircuit to model triodes, SITs and jFETs. The subcircuit makes use of the VDMOS for the main processing. Combining the jFET model with a triode model makes sense because it allows SITs to be modelled as jFETs with triode curves.

Another motivation for developing this new triode model is the lack of a suitably accurate model for very low anode voltages down to 12V [ref http://www.pmillett.com/low-voltage_tubes.htm] with good modelling with positive grid voltages. The Koren model [ref Norman Koren. "Improved vacuum tube models for spice simulations", Glass Audio , vol. 5, 1996] fails in these regions but does well in other regions [footnote [2]] and is fast and seldom encounters convergence issues. The Duncan triode model [ref Duncan Munro. Generic Triode Model V2.0 – Documentation, 1997] lacks smooth transitions in the low Va and positive Vg regions. Smooth derivatives are helpful for realistic distortion simulations.

Overview of the TriJmos subcircuit

Figure 213-A1 shows the basic TriJmos subcircuit. An equation function for source B1 converts the VDMOS square-law to a programmable power-law for triodes. Subcircuit X1 is a generic lookup table that defines the power-law curvature which changes with grid voltage which allows an easy and very close fit to measured triode curves. The Island effect is another table using B3 to scale the anode current from B1. With one table entry for every Vg curve in the Ia vs Va family it becomes easy to get a very close fit to triode curves.

Other triode parameters Kp, Mu and Vto are fixed. Triodes Mu is modelled using series voltage feedback (E1) giving the textbook triode basic relationship between grid voltage and anode current.

For SITs a third table is added to change the effective Mu with gate voltage (more in the SIT section).

1 Quasi-saturation occurs in BJTs and FETs going from the triode region to the saturation region of FETs (active region in BJTs). The VDMOS models this transition as a step change in slope. But in real FETs the transition is smooth over several volts. The gradual change in drain conductance affects distortion in some applications such as CMOS inverters in guitar overdrive effects units. Quasi-saturation is not significant when jFETs are cascoded.

2 See Adrian Immler's paper "Best of history's merged to new vacuum tube SPICE models" [SimpleSite]

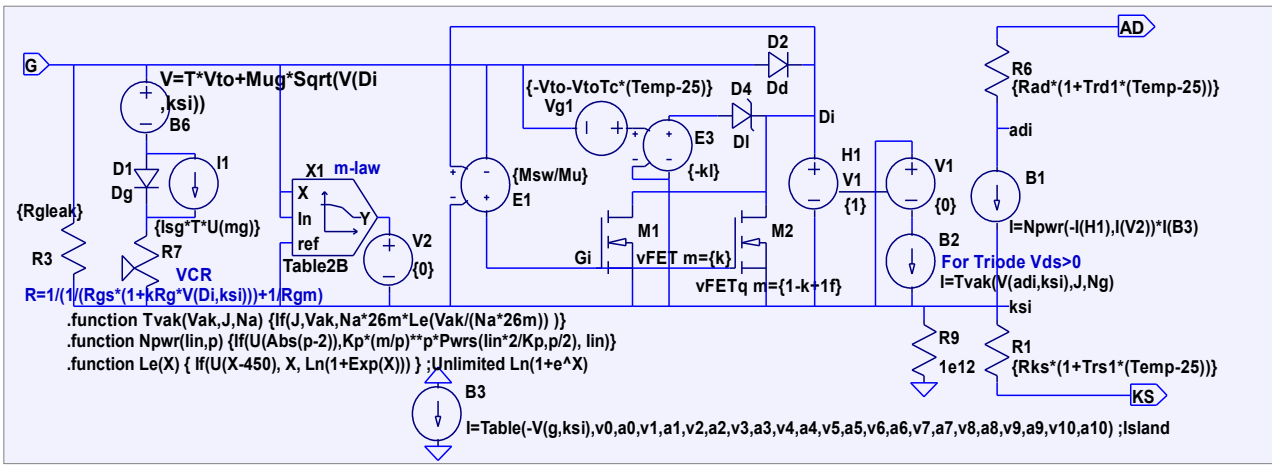

Figure 213-A1. TriJmos using the VDMOS. Triode power-law uses table X1 with B1

What else do we need? Grid current – this is modelled by a diode in series with a resistor. In triodes the diode Shockley equation has it's reverse saturation ('Is') nulled out. But for jFETs this reverse saturation is not nulled out (switch parameter mg=0 turns I1 off for jFETs).

The Island effect in triodes causes the gain to fall as gate voltage becomes large negative. The table function for the island effect can use up to 11 x,y pairs. These x,y pairs are passed from the model into the subcircuit allowing a *generic* subcircuit. The number of table pairs used can be varied to suit the triode. Only hard-to-model triodes need a large numbers of table parameters. Any unused table pairs can be left out of the model parameter list.

For triodes we need a small anode current when the anode-cathode voltage is zero – as shown in **Figure 213-A2**. This is called 'Anlauf' current. It is German – run-up for take-off.

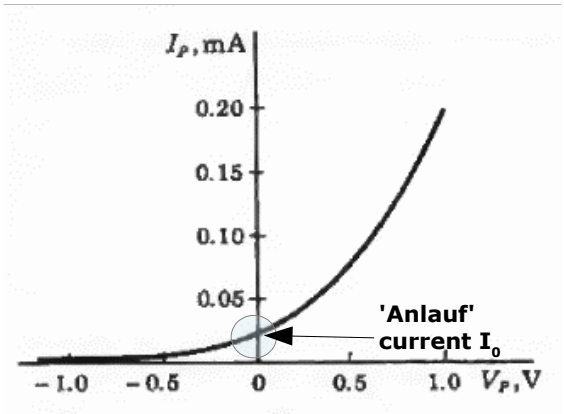

Figure 213-A2. Some thermionic diode current flow with zero anode voltage

[Ref: J Millman & C. Halkias, Electronic Devices & Circuits McGraw-Hill 1967, Fig 4.5]

Thermionic diodes and triodes differ from semiconductor diodes in that the anode current is slightly positive when the anode voltage is exactly zero [footnote[3]]. Figure 213-A2 for this unspecified triode shows the 'Anlauf' current as 25uA and in a triode this current is modulated by positive grid voltage.

Thermionic diodes and triodes generate some anode current when anode-cathode voltage is zero because of the high cathode temperature which has enough radiation energy for some

3 Unlike triodes, MOSFET's, jFETs and SITs do conduct in the 3rd quadrant (negative drain-source voltage gives a negative drain current). Apart from the parasitic body diode in MOSFET's. There's no D-S body diode in jFETs, instead G-D and G-S diodes can conduct. For jFET and triode modelling using the VDMOS the body diode series resistance parameter (Rb) is used to disable the VDMOS body diode (by setting Rb to a very large value like 1e12).

anode current with no applied voltage. So thermionic diodes and triodes act as a minuscule power source with no applied anode voltage. Whereas semiconductor diodes and transistors always sink power. In semiconductor diodes the saturation current cancels to zero when the terminal voltage is zero and this property is modelled independent of junction temperature.

For the TriJmos **triode** model we don't want any 3rd quadrant reverse current as in Figure 213-A2. A SoftPlus function transforms negative anode voltage into a positive only voltage applied to the VDMOS drain using sources B2 and H1 [footnote [4]]. The anode current at zero anode volts is then set by the SoftPlus 'N' parameter (the nonideality slope for the exponential region). Anlauf current being exponential is similar to the subthreshold current in MOSFETs – in triodes it is responsible for the low anode "knee" current with high anode voltages and large negative grid voltages.

TriJmos for modelling a jFET

For **jFETs** the 'grid' diode is now called the gate-to-source diode (D1). For jFETs there is a second gate diode – the gate-to-source diode (D2). A third gate diode D4 is a zener diode for drain-to-gate leakage current. When D2 or D3 are not needed they can be turned off by setting the diodes 'm' parameter (area scale factor) to zero [foonote[5]]. The second gate-to-drain diode is enabled by setting flag `md=1`. This flag is automatically set to 1 when the flag `Device=1` is set in the model parameters. Similarly I1 is turned off when `Device=1`, where `Device=1` is for jFETs and `Device=0` is for triodes.

For jFET drain-gate leakage (I_{GSX}) at high Vds and Tj

The standard jFET model in SPICE does not model gate-drain leakage which increases significantly at high drain-source voltages and high temperatures which requires lower input to ground 'gate-leak' resistors. Zener diode D4 with E3 and Vg1 model this effect. Series resistor of D3 (not shown is parameter "Rdl") of typically 100k ohms limits this *leakage current* above Vds of 20V to current only uA's and starting as a few pA at room temperature. This start current increases to a few nA at high temperature, **Figure 213-A3**.

Figure 213-A3 left shows the Ig vs Vds plots for the LSK389B datasheet. Left shows the TriJmos [footnote [6]].

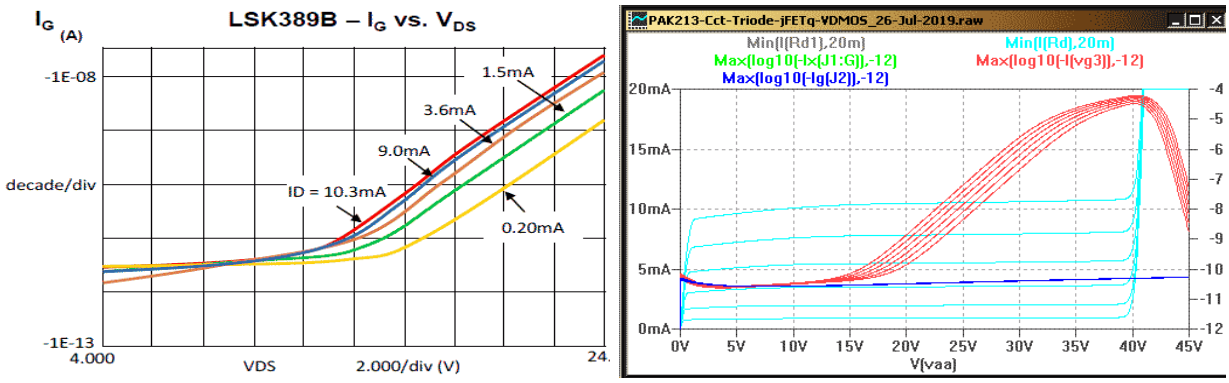

Figure 213-A3. [L] LSK389B datasheet Ig vs Vds. [R] TriJmos

Adding jFET quasi-saturation

4 A Bi current source rather than a Bv voltage source is recommended in the LTspice Help file on Behavioral sources. This Bi is converted to voltage using a dummy Voltage source (`V=0`) with an H source. Bv voltage sources can cause slow simulations and/or convergence issues in feedback loops.

5 This diode is disabled by setting the diode area to zero using code `m={md}` entered in the 'Value2' line using the Component Attribute Editor (Ctrl+Rt-clk) and this is not displaying Fig 213-A1 for clarity but it can be seen in the netlist and the subcircuit listings.

6 Breakdown can be enabled by editing the TriJmos listing, in the 2 .model scripts remove ";" to enable Bv & Nbv.

The standard SPICE jFET does not model quasi-saturation (neither does the VDMOS). Quasi-saturation is seen as a small increase in drain conductance (Gos) at low drain-source voltages voltages (1-10V) but still in the saturation (current source) region **Figure 213-A5 [R]**.

Quasi-saturation causes nonlinear distortion if/when the load line intersects the quasi-saturation region. In most amplifiers the load line does not intersects the quasi-saturation region except when clipping occurs and clipping distortion is usually ignored in amplifier specifications (also see footnote1). With quasi-saturation added to a jFET model the id vs Vds curves look closer to the actual curves as in datasheets [footnote [7]].

Quasi-saturation can be roughly modelled using two VDMOS devices in parallel. Each VDMOS is the same except for the *Mtriode* parameter. The second VDMOS has its *Mtriode* value set to a small value [footnote [8]]. With two VDMOS in parallel we want their total currents and capacitances add to that of a single device. The trick here is to scale the area of the first VDMOS by 'k' (typically 0.9) and the second VDMOS by '1-k' (typically 0.1). This trick works well with no convergence issues and there is only a small increases the simulation time.

Figure 213-A4 shows the Id vs Vgs plots for the subcircuit [L] and datasheet [R]. Quasi-saturation can be seen in the top trace from Vds of 1V to about 10V.

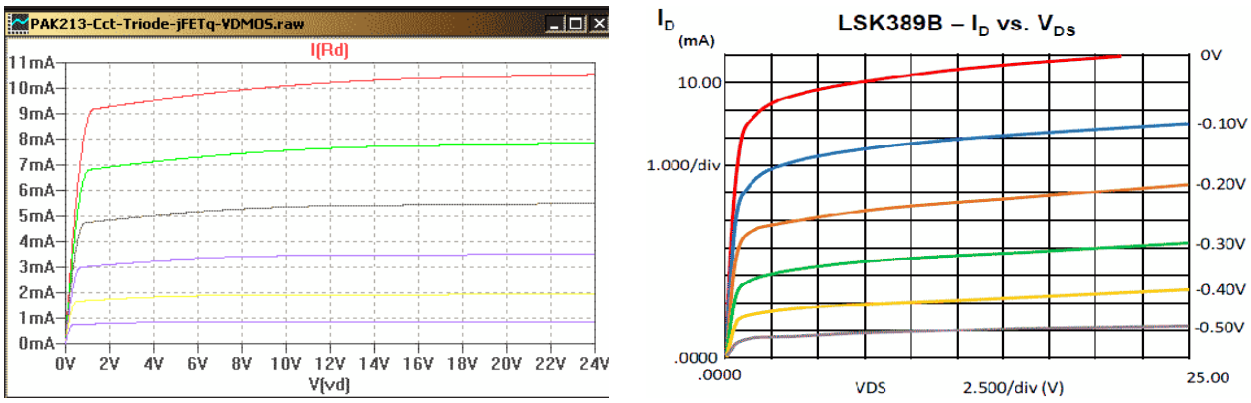

Figure 213-A4. [L] TriJmos LSK389B Ig vs Vds [R] LSK389B datasheet

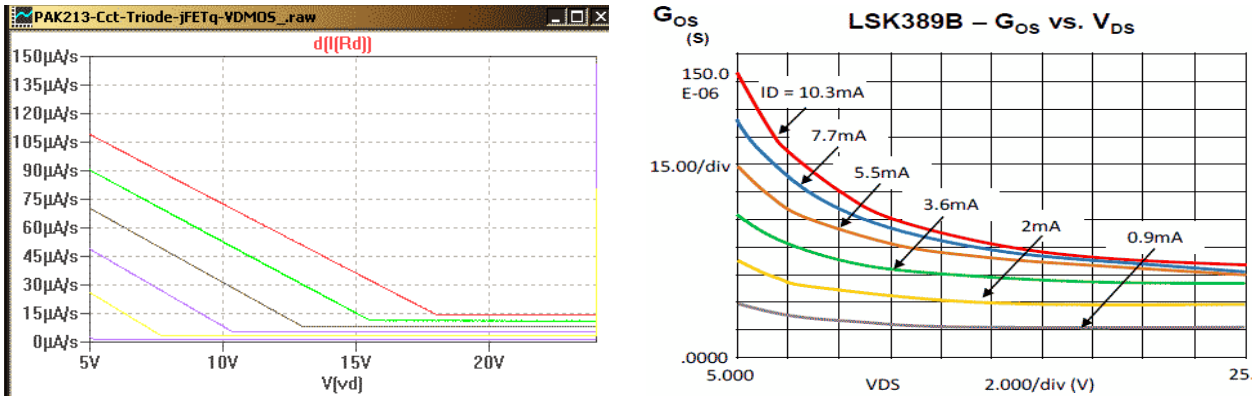

Figure 213-A5 [L] TriJmos LSK389B Gos vs Vds step 0.5V, 0 to -2.5V. [R] datasheet

In Figure 213-A5 [L] the TriJmos quasi-saturation using two VDMOS in parallel gives a linear reduction in Gos but in reality there is a *rounding* at the bottom as seen in the LSK389B Gos vs Vds curve on the right [footnote [9]].

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7 Nice for bragging rights but not that significant for most high feedback amplifier distortion simulations

8 If you can get your head around the following well and good: With the second VDMOS *Mtriode* value set to a small value you get an extended delay changing from the triode region to the saturation region while the first VDMOS is still operating in the saturation region.

9 Wouldn't it be nice if Gos rounding could be generated with two VDMOS in parallel? Well, this is done in my

Handling P-channel devices

A subcircuit **Figure 213-A6** is used to convert the N-channel version to P-channel.

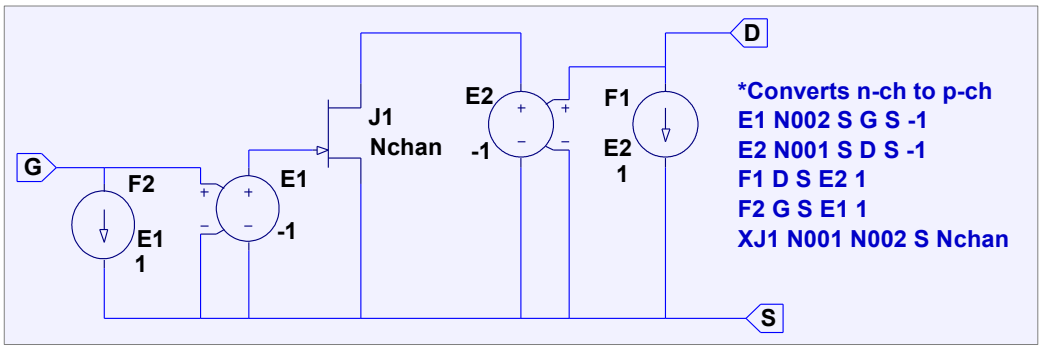


Figure 213-A6. Subcircuit converts N-channel to P-channel

This means all the modelling of a TriJmos P-channel FET is done as a N-channel. From the outside world you can't tell it is an N-channel inside behaving like a p-channel FET!

It is easier to fit parameters to all N-channel's rather than treat P-channel's differently. It makes temperature coefficient signs and threshold voltage signs less confusing and less likely to cause errors.

PART 1 – SITs – power jFETs

Modelling the SIT (power j-FET)

SITs (Static Induction Transistor's) are power jFETs. **Figure 213-A7** shows the Id vs Vds and Mu vs Vds plots for the 2SK182. The 2SK182 have an exceptionally wide Mu range with Vds – from 1 to 15.

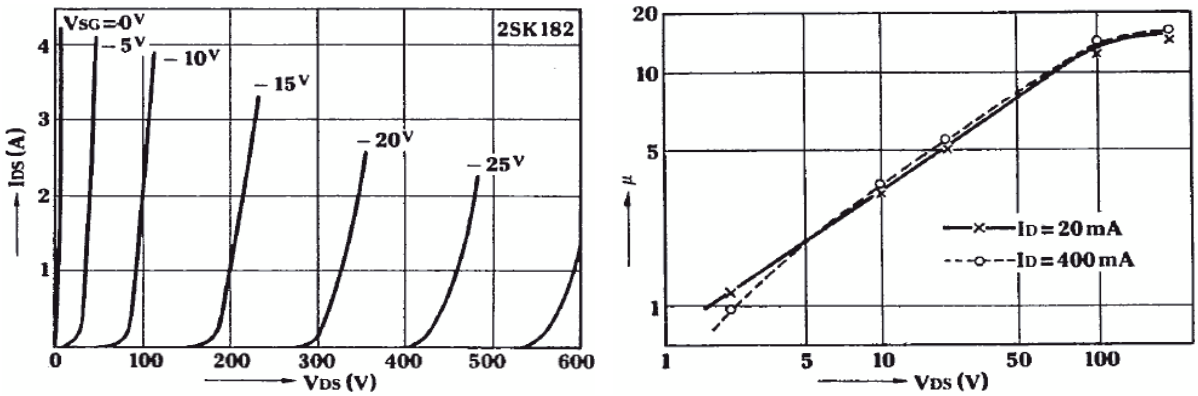


Figure 213-A7. Datasheet 2SK182 Id vs Vds and μ plots with Vds

This with range of Mu can be modelled using the TriJmos subcircuit **Figure 213-A8**. A third table (X2) is added to vary the effective Mu with anode voltage. Table X2 has the effect of changing the Vds *spacings* of the Id vs Vds family [footnote [10]]. To make table fitting easier the values used are roughly the Vds differences for low current. For example the 2SK182 from Vg=0V to Vg=-5V the curve shifts by about 20 volts on the x-axis. This gives a Mu of about 4.5, found using the first few curves with small gate voltages.

For a very large negative Vg of -30V the Mu needs to increase. The offset is not 4.5 times 30 (or 140V) but 550V. So there is a 410V *difference* and we simply enter '410V' into table X2.

updated VDMOS-Qs subcircuit. Rounding is not done for the TriJmos here to keep it is simple as possible.

10 It is not changing the actual Mu parameter but is changing the *effective* Vto parameter by the difference in Va/Mu.

Likewise for the other offset voltages. The effective Mu at Vg of -30V is (550V–450V)/(30-25)=20 (see above the datasheet Mu plot with Vds).

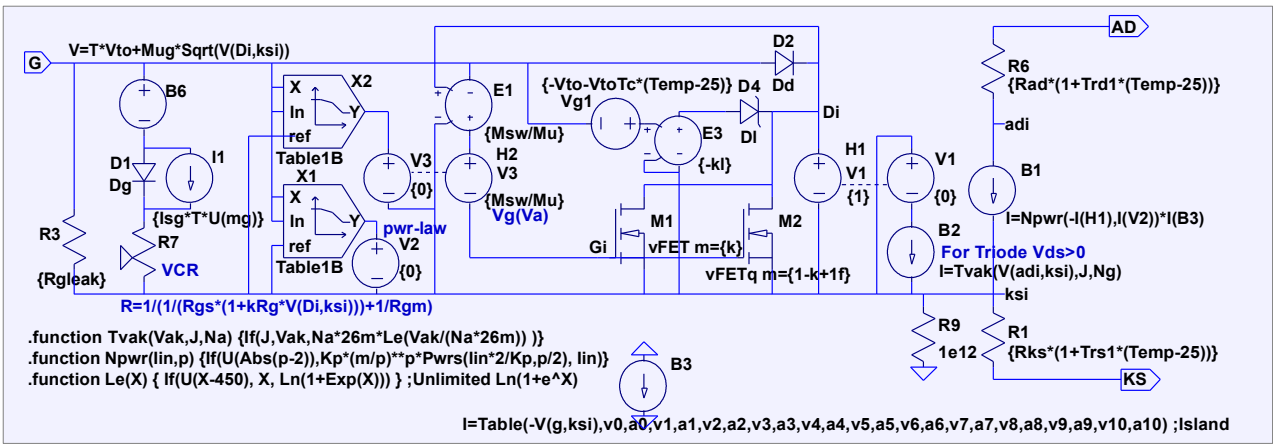


Figure 213-A8. TriJmos for SITs. Mu variation for Va is added by X2 & H2

The TriJmos 2SK182 model is shown in **Figure 213-A14**. Parameter listings for SITs are given in Appendix 3.Parameter fitting steps for SIT are given in Appendix 4.

BTW the TriJmos can model temperature but it's not covered here to reduce clutter.

TriJmos plots for some SITs

The following **Table** lists SIT devices already fitted. Small signal jFETs are covered in **Part 2**.

Power jFETs (SITs)

1. SJEP120R100 1200V 17A @100°C	2. 2SK60 Sony SIT
3. 2SK77 Yamaha 250V 10A	4. 2SK82
5. 2SK180 Tokin SIT	6. 2SK182 Tokin SIT
7. SIT-1	8. Spare

1: SJEP120R100 SIT

The SemiSouth SJEP120R100 has a comprehensive subcircuit which includes temperature effects. [ref https://www.diyaudio.com/forums/pass-labs/179116-semisouth-spice-models-post2843791.html 2012]
The TriJmos plots are to within a few percent of the SemiSouth subcircuit and datasheet.

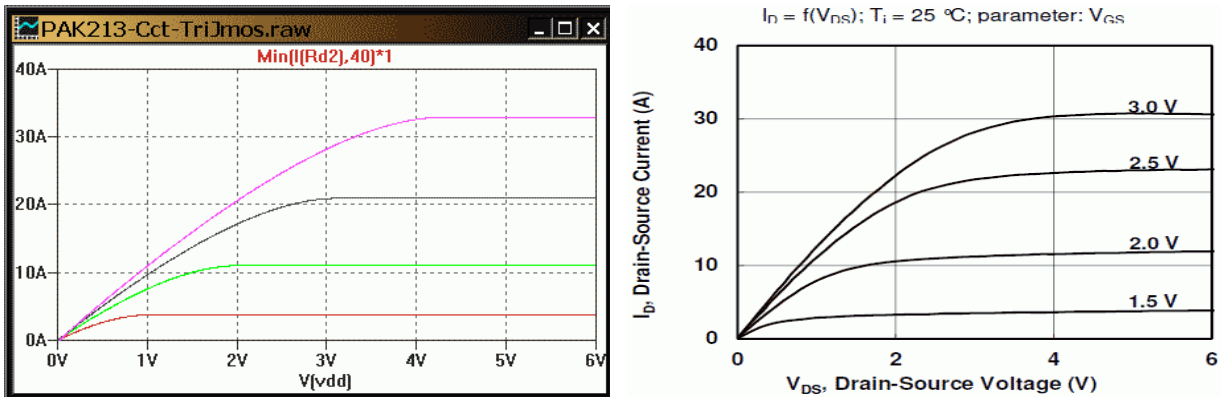
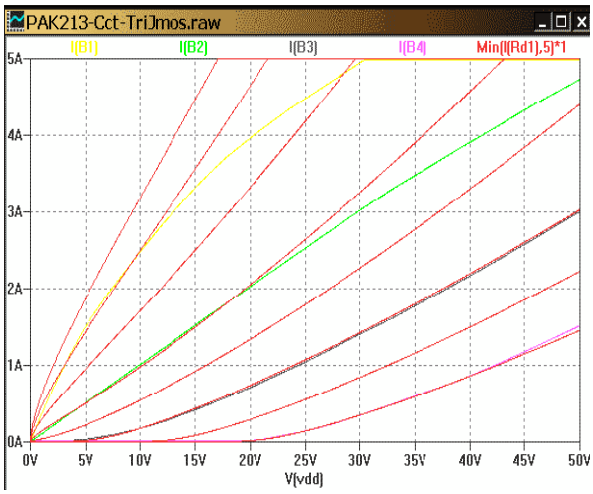


Figure 213-A9. [L] TriJmos SJEP120R100 Vg 1.5, 2, 2.5, 3 [R] datasheet

2: 2SK60 Sony SIT 5A 170V



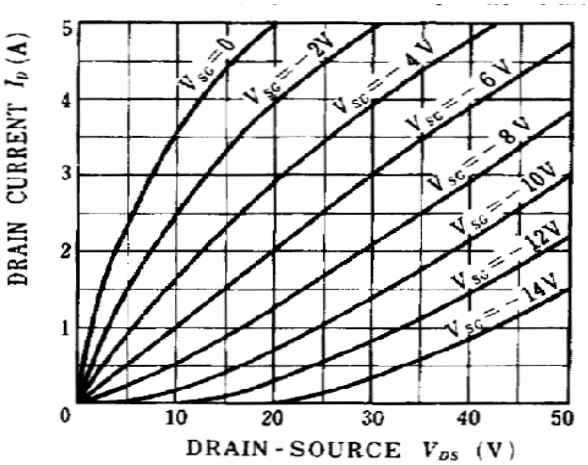
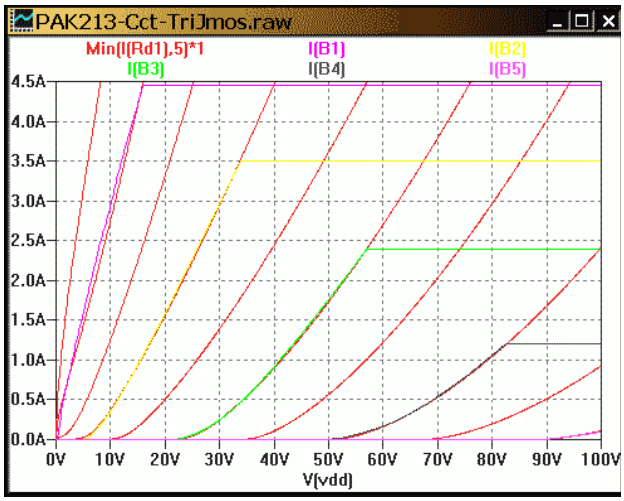


Figure 213-A10 [L] TriJmos 2SK60, Vg 0 -2 -4 -6 -8 -10 -12 -14V [R] datasheet

3: 2SK77 Yamaha SIT 10A 250V



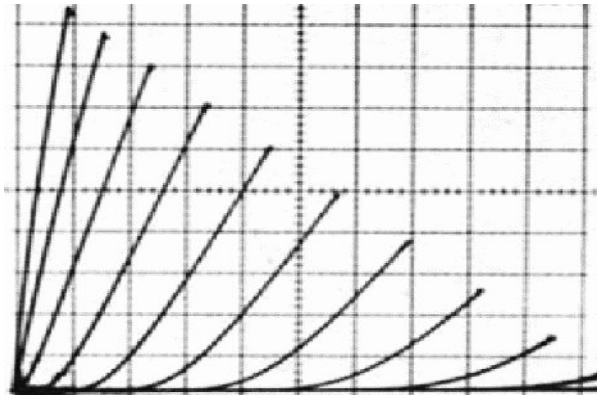
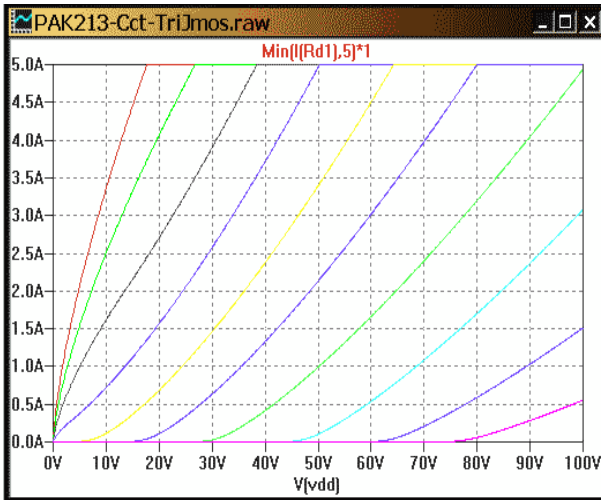


Figure 213-A11 [L] TriJmos 2SK77 Vg 10 steps -1, -10V [R] datasheet 0.5A, 10V/div

4: 2SK82 SIT



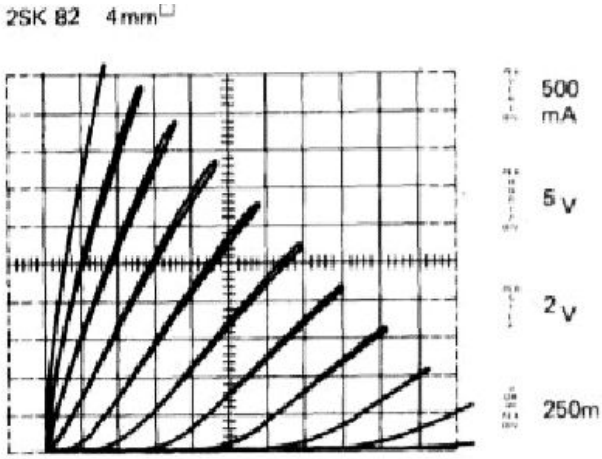


Figure 213-A12. [L] TriJmos 2SK82, Vg 0V to -18V, 2V steps [R] datasheet

5: 2SK180 SIT (see 2SK182 as no plots available. Scale 2SK182 Kp by 0.33)

Figure 213-A13. 2SK180 no plots available

6: 2SK182 SIT

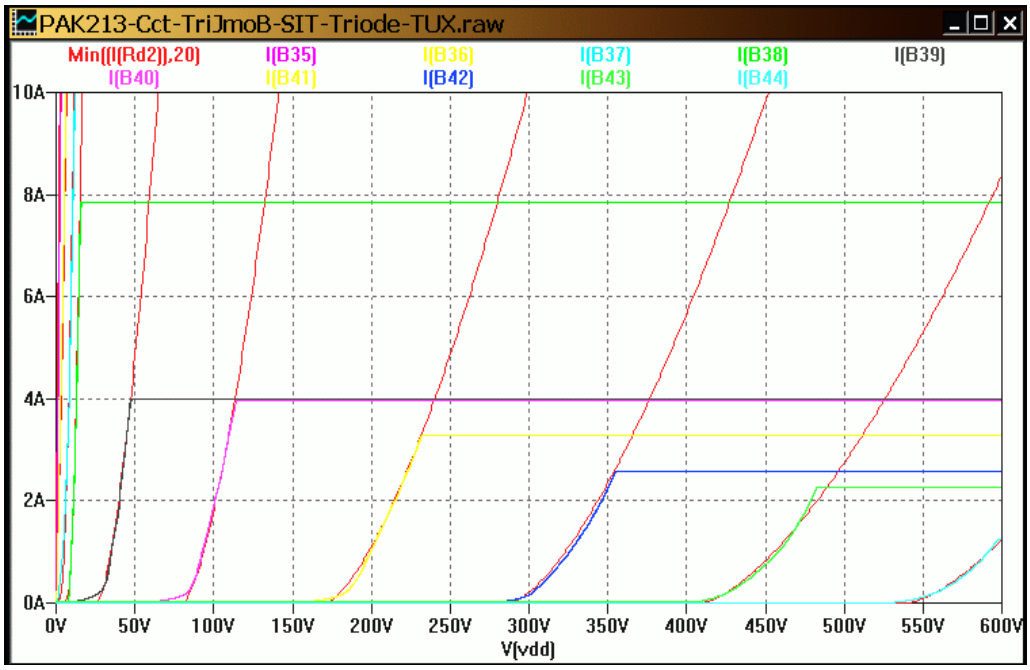
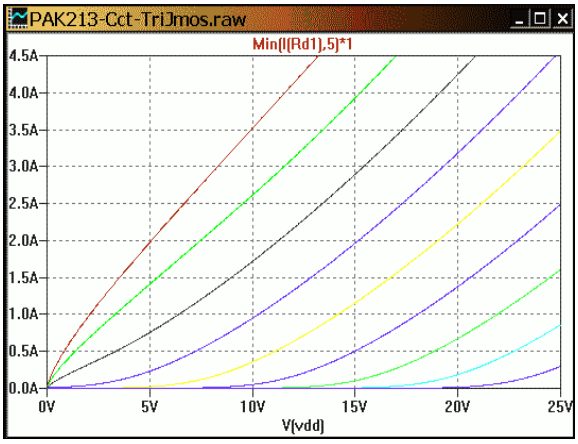


Figure 213-A14. TriJmos 2SK182 Red Vg 0 -1 -3 -5 -10 -15 -20 -25V -30V. Datasheet

7: SIT-1 power jFET



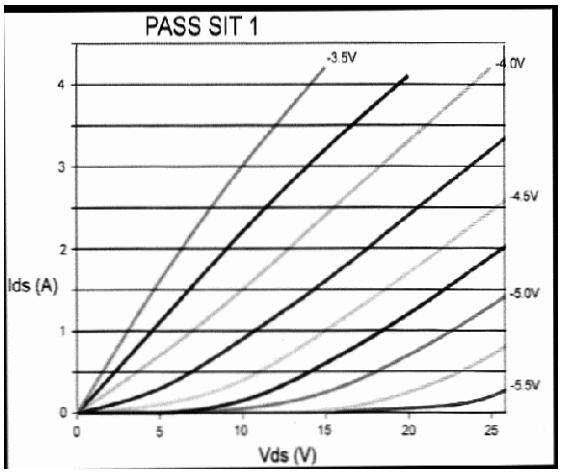


Figure 213-A15 [L] TriJmos SIT-1 Vg -3.5V to -5.5V?, [R] Linear Audio V4 p71

8: Spare

Figure 213-A16. [L] TriJmos spare. [R] Datasheet

How to use TriJmos Model parameters

Normally you use the 'Cell' text based subcircuits with the model text code in a text file with an .include <filename>.txt card on your circuit. You change the "Prefix" flag to "X" (see below).

If you want to debug or modify the model and recompile a new version then you need to use the 'Block' circuit based subcircuit. Appendix 9 covers the steps to add parameters into each instance using the Attribute Editor. If you are new to LTspice and subcircuits, when you need to change a jFET symbol to accept a part *that uses a subcircuit* you need to change the "**Prefix**" flag from "JN" to either: A) "X" (for a 'Cell' subcircuit), or B) nothing (for a 'Block' subcircuit). To access the Component Attribute Editor use Ctrl+RtClk with the cursor on a new jFET.

Parameter fitting steps are at the end of the model listings.

PART 2 – Small signal jFETs

Model plots for some small signal jFETs

The following **Table** lists devices I have fitted for this paper.

Small signal jFETs

9. LSK389B (comp is 2SJ109)	10. LSK489B
11. LSJ689B (2SJ109) p-ch	12. BF545B (was BF245GR), 2SJ103
13. LSK170B	14. LSJ74B p-ch
15. 2SK932-23	16. Spare

9. LSK389B n-jFET

The LSK389B is shown as **Figure 213-A17**. Blue is the standard model.

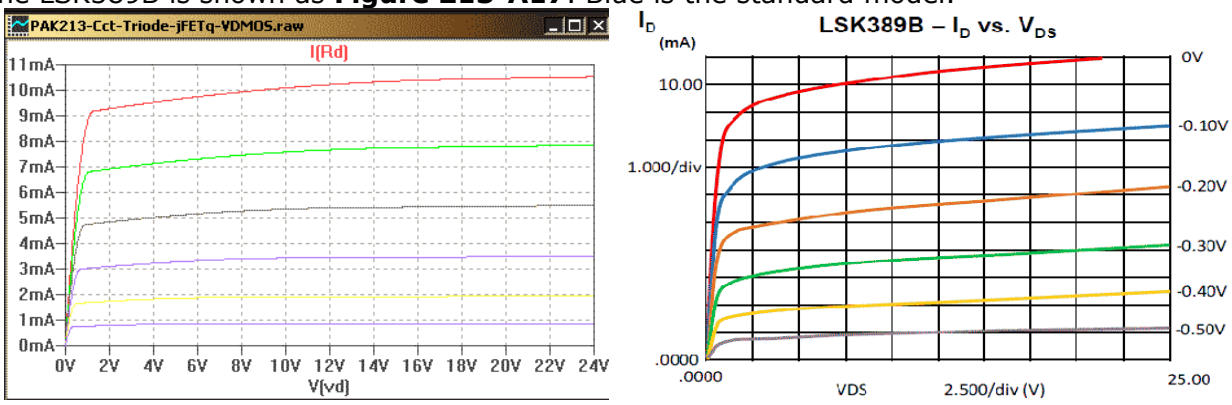


Figure 213-A18 [L] TriJmos LSK389B Subcircuit. [R] Datasheet Vg stepped

10. LSK489B n-jFET

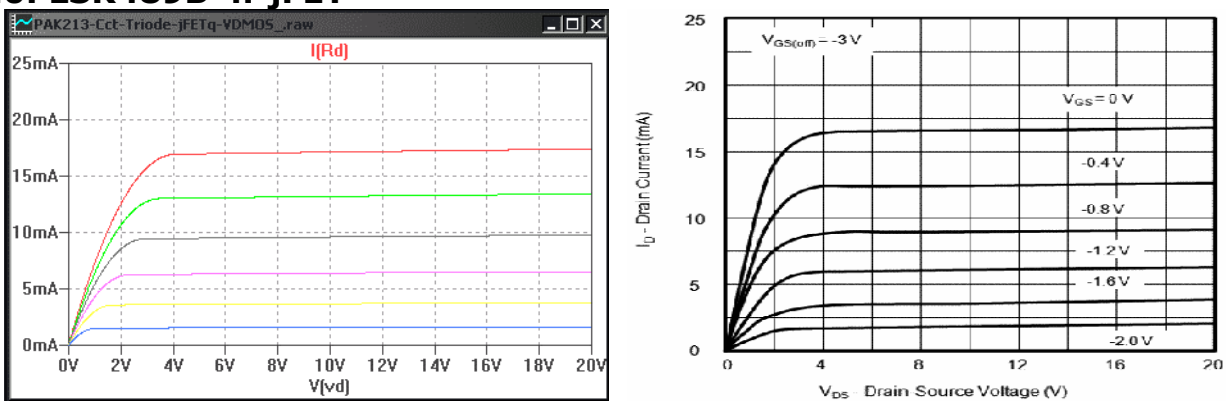


Figure 213-A19 [L] TriJmos LSK489B Subcircuit. [R] Datasheet Vg stepped

11. LSJ689B p-jFET

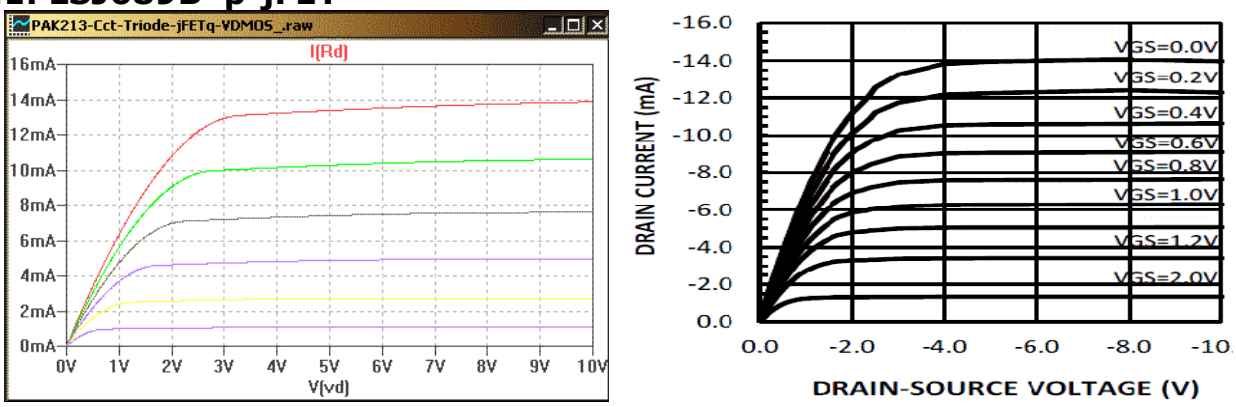
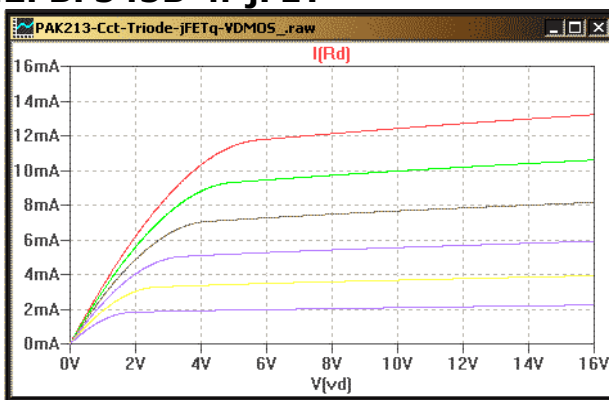


Figure 213-A20 [L] TriJmos LSJ689B Subcircuit. [R] Datasheet Vg stepped

12. BF545B n-jFET



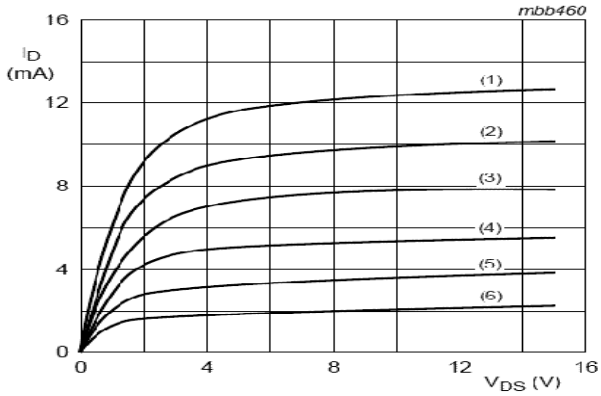
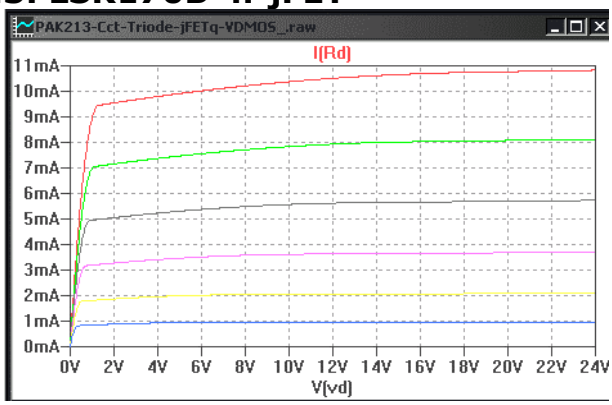


Figure 213-A21 [L] TriJmos BF545B Subcircuit. [R] Datasheet Vg 0 to -2.5V

13. LSK170B n-jFET



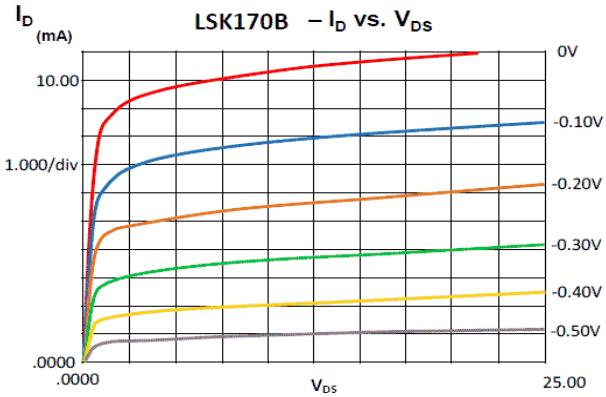
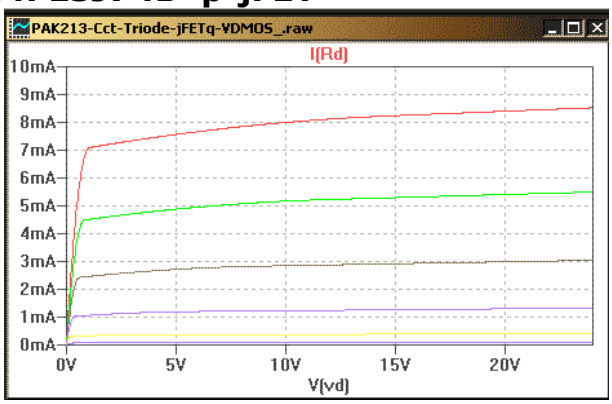


Figure 213-A22 [L] TriJmos LSK170B Subcircuit. [R] Datasheet Vg stepped

14. LSJ74B p-jFET



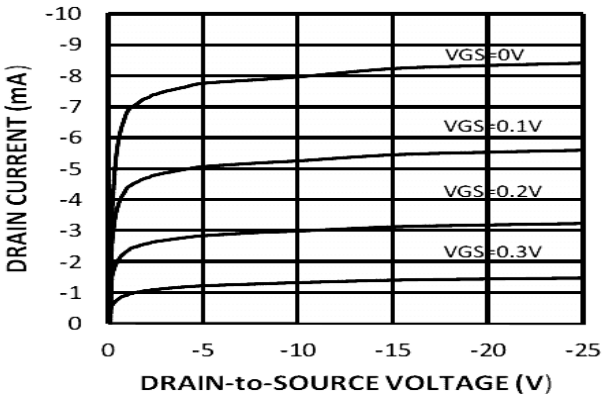


Figure 213-A23. [L] TriJmos LSJ74B Subcircuit. [R] Datasheet Vg stepped

15. 2SK932-23 n-jFET

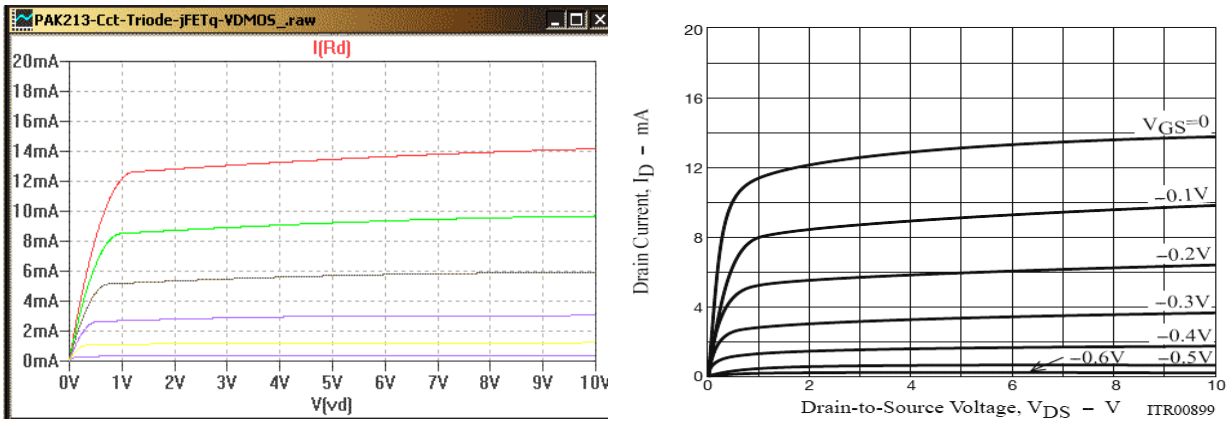


Figure 213-A24 [L] TriJmos 2SK932-23 Subcircuit. [R] Datasheet Vg stepped

16. Spare

This is deliberately left blank

Figure 213-A25. Spare

Noise parameters for small signal jFETs using the VDMOS subcircuit

Noise simulations can be performed for a subcircuit in LTspice using the card:

```
.noise V(d1) Vg1 oct 100 1 1Meg
```

where V(d1) is the drain node of the subcircuit and Vg1 is the name of the signal source feeding the jFET amplifier. The small signal value is set to 1V for the signal source like for the `.ac` card. Click on the d1 node to display the noise density plot or select "V(onoise)" trace in Plot Settings **Figure 213-A26**. Ctrl+Left-Clk integrates to give the noise voltage over the frequency range.

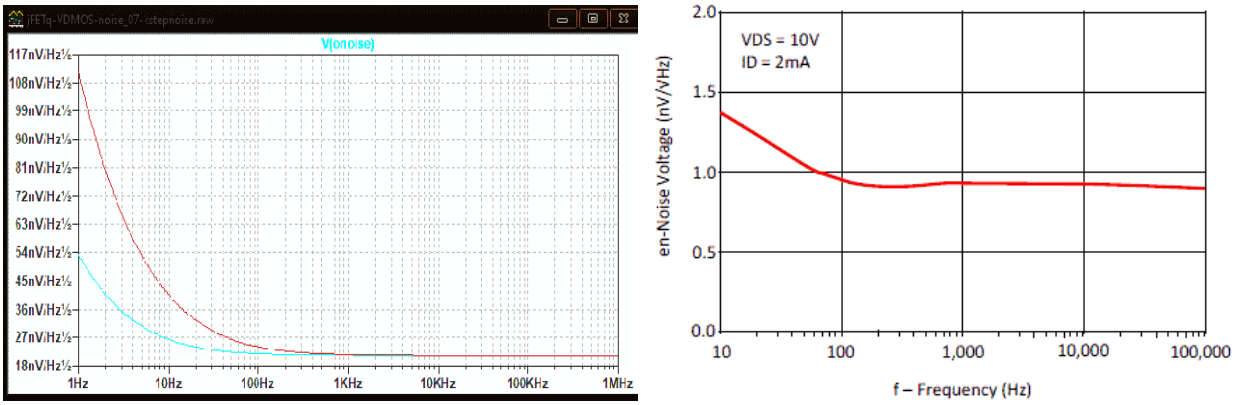


Figure 213-A26. [L] TriJmos 2SK932-23 with Kf stepped 1e-29 and 5e-29, Af=1 [R] LSK389 datasheet noise density plot

Parameter Kf sets the level of the 1/f noise and Af shifts the 3dB intersection of the 1/f with the broadband noise. There appears to be a bug in the VDMOS noise simulations for LT-XVII as of Aug 2019 [footnote [11]].

Until the VDMOS noise is working properly it is best to use the standard jFET for noise simulations. Convert the relevant subcircuit parameters as follows [footnote [12]]:

```
VTO=-|Vto| BETA=Kp/2 RS=Rks RD=Rad IS=Isd
+ CGD=Cgdmin CGS=Cgs BETATC=Bex + 1 VTOTC=-|VtoTc|
```

11 The noise card does not work at all for the VDMOS in LT-IV. The noise card does work at all for the VDMOS in LT-XVII but only when the 'Normal' engine is used (set in Control Panel>SPICE>Engine Solver>Normal). Also the VDMOS Kf parameter needs a value of 1e-29 to give similar noise to the standard jFET with Kf=1e-18 – this difference is an assumed to be a bug. An Af=1 gives the same effect in both jFET and VDMOS.

12 There are differences in the Vto sign between p- and n- for the VDMOS and the jFET. The jFETs VTO is always negative for p- and n- devices (but in reality they are opposite sign in a circuit). This difference also applies to the VTOTC and BETATC parameters for the jFET.

TriJmos Parameter listings for the above small signal jFETs

Parameter listings for jFETs are given in Appendix 1.Parameter fitting steps for jFETs are given at the end of Appendix 2.

PART 3 Triodes

17. 12AT7/ECC81	18. 12AU7/ECC82
19. 12AX7/ECC83	20. Spare

TriJmos modelling triode Mu variation

For triodes Mu *variation* determines the majority of the nonlinear distortion. Mu variation with Vg (Island effect) can be modelled as a reduction in the Kp with more negative grid voltages. The Island effect also increases the curvature of Ia vs Va plots with more negative grid voltages; this can be modelled as an increasing power-law with more negative grid voltages. The variation in power-law is from about 1.5 with no Island effect to about 2 with large negative grid voltages and then it stays nearly constant for even larger negative grid voltages.

TriJmos plots for some triodes

17. 12AT7/ECC81

Figure 213-A27 shows plots for the 12AT7 model fitted to measured data (courtesy of Adrian Immler, thanks so much! [Site 12AT7].

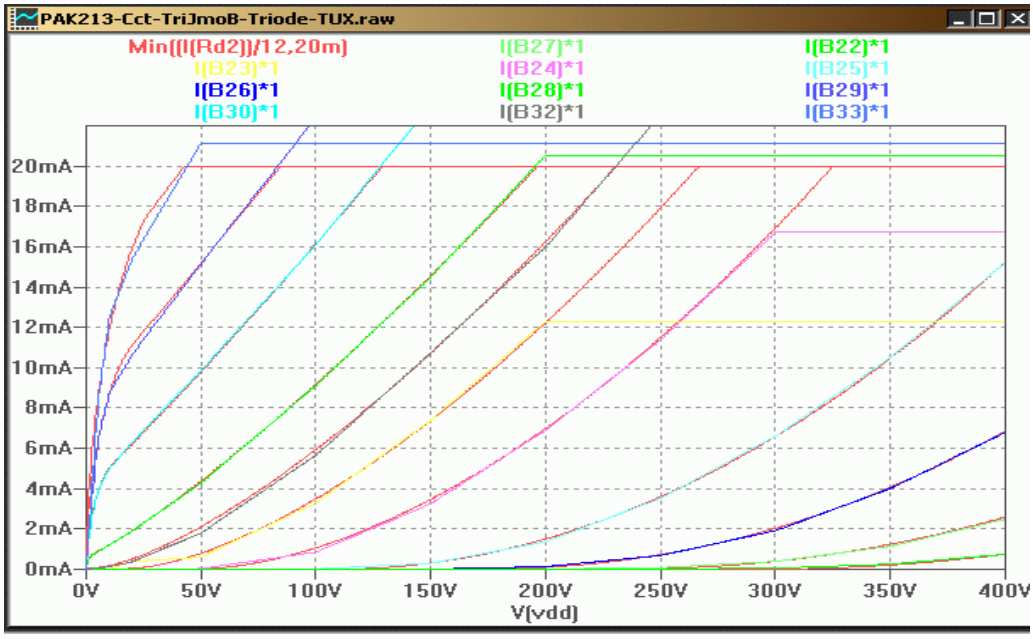


Figure 213-A27 [L] TriJmos 12AT7/ECC81, Vg=+3,2,1,0,-0.5,-1,-2 to -8, -10V
Measured data courtesy Adrian Immler Site 12AT7

18. 12AU7/ECC82

Figure 213-A28 show 12AU7 plots fitted to datasheets.

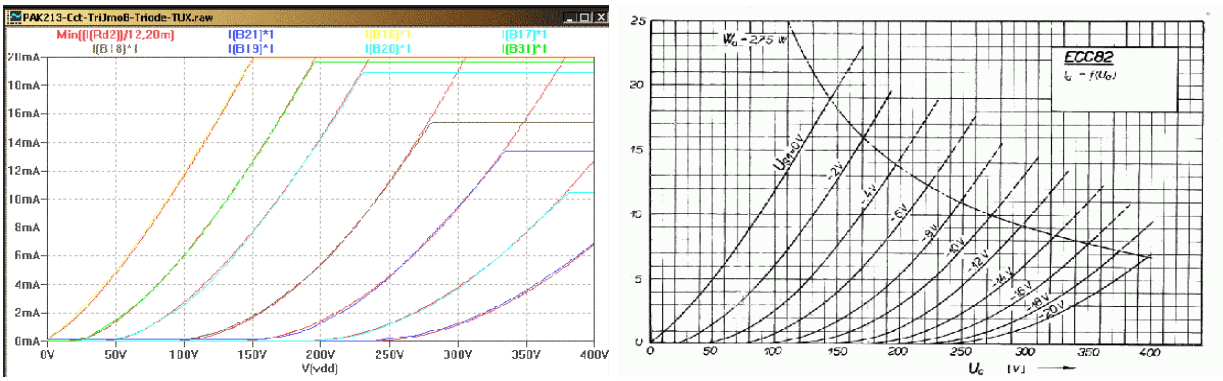


Figure 213-A28 [L] TriJmos Triode 12AU7/ECC82. [R] Datasheet ECC82

18. 12AX7/ECC83

Figure 213-A29 show 12AX7 plots fitted to datasheets.

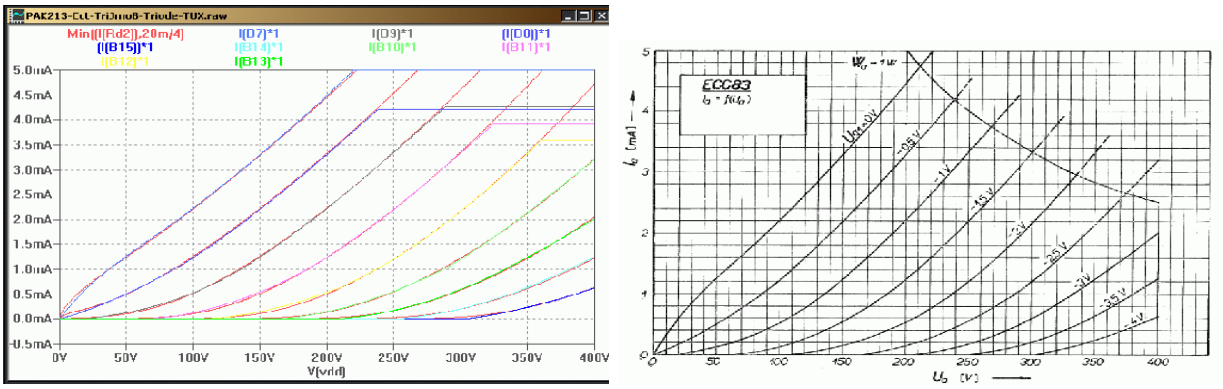


Figure 213-A29 [L] TriJmos Triode 12AX7/ECC83. [R] Datasheet ECC83

Emission saturation has not been modelled since in most audio applications operation is not emission limited. However some aged tubes and triodes operating at reduced filament current may need saturation limiting effects.

TriJmos Parameter listings for Triodes

Appendix 5 has parameter listings for Triodes. Check my SPICE model page for updates. Parameter fitting steps for Triodes are given at the end of Appendix 6.

Speed tests

Speed tests were done comparing the TriJmos to the Koren and Duncan models but it was discovered that most of the time was for updating the video display so no meaningful sped tests are available at this time.

Main TriJmos generic subcircuit listing

Appendix 7 has the generic subcircuit listing. Check my SPICE model page for updates.

Getting started using the TriJmos

A demo circuit can be download. Appendix 10 covers how to use the jig.

Summary:

This new subcircuit adds important effects seen in jFETs and Triodes including:

- jFET gate-drain leakage current (I_{GSX}) changing with Vds and temperature
- Quasi-saturation is significant for most small-signal jFETs
- Noise parameters are included

- Triode Island effect is accurately and easily fitted using table parameters
- Triode grid current includes modulation by anode voltage
- All these effects are built into one generic subcircuit to model the 3 devices: Triodes, SITs and jFETs.
- Default parameters allow unused parameters to be left undefined as per SPICE.

I hope you find this useful. Please let me know if you find any mistakes, have any suggestions or need any assistance. My Contact is on my website (link at the top).

Add. My other subcircuits

My subcircuit to add quasi-saturation to the VDMOS is called the **VDMOS-qs**.
Another subcircuit adds electrothermal effects to the VDMOS and it is called the **VDMOS-Th**.
An electrothermal with quasi-saturation called the **VDMOS-QsTh** is also available.

---------- ----------

Appendix 1-11:

For updates check my SPICE model page
Archived at https://web.archive.org/ enter "https://paklaunchsite.jimdo.com/"
Also check https://diyAudio.com/forums/software-tools

Appendix 1: TriJmos Parameter listings for small-signal jFETs

1.1 LSK389 jFET

```
*TriJmos 1v2 (c) Ian Hegglun Sep 2019
.SUBCKT LSK389B  D  G  S
X1  D G S TriJmos params:Device=1 Vto=-0.64 Kp=70m k=0.85
+ Ksubthres=0.1 Mtriode=0.5 kt=60m Lambda=2m
+ Rks=10 Rad=8 VtoTc=-1m Bex=-2 Trs1=3m Trd1=3m
+ Cgdmax=20p Cgdmin=5p a=1 Cgs=25p Cjo=25p Rg=10 kf=2e-29 Af=1
+ Isg=30f Bvdl=16 Ibvl=1p Nbvdl=50 Rdl=100k kl=10 ml=1 ;g-d leak diode
.ENDS
```

1.2 LSK489 jFET

```
*TriJmos 1v2 (c) Ian Hegglun Sep 2019
.SUBCKT LSK489B  D  G  S
X1  D G S TriJmos params:Device=1 Vto=-2.65 Kp=9m k=0.95
+ Ksubthres=0.1 Mtriode=0.6 kt=80m Lambda=1m
+ Rks=40 Rad=8 Rds=1G VtoTc=-1m Bex=-1.8 Trs1=3m Trd1=3m
+ Cgdmax=20p Cgdmin=3p a=1 Cgs=4p Cjo=4p Rg=10 kf=2e-29 Af=1
```

```
+ Isg=30f Bvdl=16 Ibvl=1p Nbvdl=50 Rdl=100k kl=10 ml=1 ;g-d leak diode
.ENDS
```

1.3 LSJ689 p-jFET

```
*TriJmos 1v2 (c) Ian Hegglun Sep 2019
.SUBCKT LSJ689B  D  G  S
E1 N002 S G S -1 ; Nchan->Pchan
E2 N001 S D S -1
F1 D S E2 1
F2 G S E1 1 ;now use Nchan params
X1  N001 N002 S LSJ689Bn
.ENDS
*TriJmos 1v2 (c) Ian Hegglun Sep 2019
.SUBCKT LSJ689Bn  D  G  S
X1  D G S TriJmos params:Device=1 Vto=-2.55 Kp=8m k=0.85
+ Ksubthres=0.2 Mtriode=0.8 kt=200m Lambda=0.6m
+ Rks=50 Rad=20 VtoTc=-2.5m Bex=-1.5 Trs1=3m Trd1=3m
+ Cgdmax=16p Cgdmin=3p a=1 Cgs=20p Cjo=20p Rg=10 kf=2e-29 Af=1
+ Isg=30f Bvdl=16 Ibvl=1p Nbvdl=50 Rdl=100k kl=10 ml=1 ;g-d leak diode
.ENDS
```

1.4 BF545B (was BF245) jFET

```
*TriJmos 1v2 (c) Ian Hegglun Sep 2019
.SUBCKT BF545B  D  G  S
X1  D G S TriJmos params:Device=1 Vto=-3.8 Kp=2.7m k=0.95
+ Ksubthres=0.1 Mtriode=0.7 kt=300m Lambda=20m
+ Rks=80 Rad=60 VtoTc=-1m Bex=-1.8 Trs1=3m Trd1=3m
+ Cgdmax=1p Cgdmin=0.8p a=1 Cgs=2p Cjo=2p Rg=10 kf=2e-29 Af=1
+ Isg=0.2f Bvdl=16 Ibvl=1p Nbvdl=50 Rdl=100k kl=10 ml=1 ;g-d leak diode
.ENDS
```

1.5 LSK170B jFET

```
*TriJmos 1v2 (c) Ian Hegglun Sep 2019
.SUBCKT LSK170B  D  G  S
X1  D G S TriJmos params:Device=1 Vto=-0.65 Kp=70m k=0.85
+ Ksubthres=0.1 Mtriode=0.5 kt=60m Lambda=2m
+ Rks=10 Rad=8 VtoTc=-2.5m Bex=-1.5 Trs1=3m Trd1=3m
+ Cgdmax=20p Cgdmin=5p a=1 Cgs=25p Cjo=25p Rg=10 kf=2e-29 Af=1
+ Isg=10u Bvdl=16 Ibvl=1p Nbvdl=50 Rdl=100k kl=10 ml=1 ;g-d leak diode
.ENDS
```

1.6 LSJ74B p-jFET

```
*TriJmos 1v2 (c) Ian Hegglun Sep 2019
.SUBCKT LSJ74B  D  G  S
E1 N002 S G S -1 ; Nchan->Pchan
E2 N001 S D S -1
F1 D S E2 1
F2 G S E1 1 ;now use Nchan params
X1  N001 N002 S LSJ74Bn
.ENDS
*TriJmos 1v2 (c) Ian Hegglun Sep 2019
.SUBCKT LSJ74Bn  D  G  S
X1  D G S TriJmos params:Device=1 Vto=-0.40 Kp=160m k=0.85
+ Ksubthres=0.1 Mtriode=0.35 kt=60m Lambda=7m
+ Rks=12 Rad=8 VtoTc=-1m Bex=-1.8 Trs1=3m Trd1=3m
+ Cgdmax=90p Cgdmin=25p a=1 Cgs=100p Cjo=100p Rg=10 kf=2e-29 Af=1
+ Isg=30f Bvdl=16 Ibvl=1p Nbvdl=50 Rdl=100k kl=10 ml=1 ;g-d leak diode
.ENDS
```

1.7 2SK932-23 n-jFET

```
*TriJmos 1v2 (c) Ian Hegglun Sep 2019
.SUBCKT 2SK932-23  D  G  S
X1  D G S TriJmos params:Device=1 Vto=-0.50 Kp=150m k=0.85
+ Ksubthres=0.1 Mtriode=0.4 kt=80m Lambda=3m
+ Rks=5 Rad=5 VtoTc=-1m Bex=-2 Trs1=3m Trd1=3m
+ Cgdmax=10p Cgdmin=3p a=1 Cgs=10p Cjo=10p Rg=10 KF=1e-29 AF=1
+ Isg=30f Bvdl=16 Ibvl=1p Nbvdl=50 Rdl=100k kl=10 ml=1 ;g-d leak diode
.ENDS
```

1.8 SPARE

Appendix 7 has the generic TriJmos subcircuit listing.

Appendix 2: TriJmos Parameter fitting steps for small-signal jFETs

Fitting parameters is best done by starting with a Id vs Vgs plot using a jig. If you have a datasheet or bench test then set the Vg range to about that of the Id vs Vgs plot. Set the Vds to the datasheet value.

If you have an existing jFET model you can glean some of the parameters [footnote 5] using:

```
VTO=-|Vto| BETA=Kp/2 RS=Rks RD=Rad IS=Isd
+ CGD=Cgdmin CGS=Cgs BETATC=Bex + 1 VTOTC=-|VtoTc|
```

Check this comprehensive library of manufacturers posted by Ludus Tonalis 26 Mar 2019 [https://www.diyaudio.com/forums/software-tools/331978-spice-database-diyaudio-post5741272.html]. Linear Systems models can be accessed here http://www.linearsystems.com/lsdata/spicemodel/.

If you don't have any existing models to start from then use the following:

1. The Vto is set to the x-intercept (approximate will do).
2. Start with Rks=0 (RS in jFETs) then an approximate value for Kp is the current at where Vg is 1V above Vto. Some jFETs you need to extrapolate to get Id at 1V above Vto.
3. If you have a gm (gfs) plot then this can give an idea for Rks (RS in jFETs). Plot d(Id) vs Vgs and look at the following:
   a) The initial slope on your plot compared to the datasheet gm curve – change your Kp up or down to match the initial slope, and
   b) How curved the gm is at higher Vgs – change your Rks up or down to match the slope rounding at higher Vgs.
   Most datasheets seem to plot gfs against Id – so can change your x-axis variable to I(R1) (where R1 is a drain current sampling resistor set to a low value of 1m or 1u ohms).
4. Back to a Id vs Vgs plot. You should now have a fairly good values for Id over the range of Vgs – check at say 10% of Idmax (Idss for jFETs), 30% and 100%.
5. If you have a log(Id) vs Vgs datasheet plot then check the slope in the subthreshold region – change Ksubthres *if* it is much different to 100mV per decade of Id (the default value). If it is say, 150mV per decade, then change Ksubthres to 150m. No need for high accuracy for this.
6. Change to a Id vs Vds plot with Vg steps same as the datasheet. Look at what Vds the triode region ends for say the 50% Id step curve. This is where the curve changes from a quadratic curve to a straightish line. Change Mtriode to get the same ending Vds (reducing from default of 1 will push the ending Vds higher). No need for high accuracy at this stage.
7. Look at the 100% Id curve initial slope. Change your Rad (RD in jFETs) to roughly match this slope. Alter Mtriode to match your ending Vds since Rd affects Mtriode.
8. Look at the 100% Id curve high Vds slope. Is it curved or straight? If it is slightly curved at medium Vds then straight at high Vds you need some quasi-saturation. If it is straight throughout then no need for quasi-saturation, just use Lambda to get the right slope. Increasing Lambda also scales up the Id where it changes from triode to saturation – so increasing Lambda from 0 to 10m will require a reduction in Kp (maybe by 10%). If you need quasi-saturation then Lambda can be fairly small and initially set to say 1m or 2m then fit for quasi-saturation.
   Look at the 100% Id curve and use the % Id at the end of triode region for parameter "k" (eg 90% Id use k=0.9). Change "kt" so the quasi-saturation region ends at the approximate Vds of the datasheet (eg use the 50% Id curve high Vds to see this end point).
   Start with kt=100m – increasing kt reduces the Vds for ending quasi-saturation. Kp may need changing. Lambda can now be trimmed – use the 50% Id curve slope at high Vds after the end point for quasi-saturation. Kp may need changing (yet again).
9. You should now have most of the main parameters fairly close to final. The next stage

is temperature coefficients, mainly for Vto and Kp. If you have a Id vs Vgs datasheet plot with stepped temperatures then change VtoTc and Bex to get a similar crossing point, the zero temp co point (ZTC). Bex is negative in the range of -1 to -2.5 (default is -1.5). VtoTc is negative for n-channel and positive for p-channel (unlike standard SPICE jFETs).

10. Choose capacitance values for Cgs, Cgdmin and Cgdmax where Cgs=Ciss and 10. Cgdmin=Crss (both at higher Vds), Cgdmax≈2×Cgdmin or 3×Cgdmin seems OK for a jFET. (Cjo does not need to be defined since it is mostly from the body diode in the VDMOS which is disabled and by default the subcircuit sets Cjo to Cjo=Cgs to avoid raising the 'undefined parameter' error).

11. Choose gate diode values from a datasheet plot of Ig else use the I_{GSS} value (gate-source leakage). If no Ig data is available then use the default Is is the same as SPICE Is=1e-14 (10fA) which is in the ball-park for small and large jFETs.

Alternatively find a similar jFET that has a datasheet with an Ig plot or I_{GSS} value. Plot log10(Ig) vs Vgs and change the Isg parameter (IS in jFETs) to get Ig passing though the datasheet value at the same Vgs.

If you want to model drain-gate diode leakage current (I_{GSX}) then you need a Ig vs Vds plot – change the parameters Bvdl, Ibvl, Nbvdl, Rdl, kl, and set ml=1 (defaults are Bvdl=16, Ibvl=1p, Nbvdl=50, Rdl=100k, kl=10, ml=0). These give a changing amount of drain-gate diode leakage current (I_{GSX}) with drain-source voltage using a zener diode (Bvdl, Ibvl, Nbvdl) with a high value series resistance (Rdl) and a voltage amplification factor (kl) to set the Id offset with Vgs changes.

Plot Ig vs Vds to see if the default values are satisfactory and tweak them if needed.

6. Noise parameters can be checked by plotting "V(onoise)" as described above.

We're about done. You can add the model to your library – see the section "How to use the above Model parameters" in Part 1. It's now ready to use it in your amplifier.

---------- ----------

Appendix 3: TriJmos Parameter listings for SITs

3.1. SJEP120R100

```
*TriJmos 1v5 (c) Ian Hegglun Dec 2019
.SUBCKT SJEP120R100  D  G  S
X1  D G S TriJmos params:Device=1 Vto=0.9 Kp=24 Mu=100
+ Rks=14m Rad=45m  Ksubthres=100m Mtriode=0.7 Msw=1
+ VtoTc=-2m Bex=-4.1 Trs1=10m Trd1=20m
+ Cgdmax=1000p Cgdmin=40p a=1 Cgs=670p Rg=6
+ Isg=1f Ng=3.4 Egg=3.7 Rgs=0.7*(1-2.4m*(Temp-25)) ;gate diode
.ENDS
```

3.2 2SK60 SIT

```
*TriJmos 1v5 (c) Ian Hegglun Dec 2019
.SUBCKT 2SK60  D  G  S
X1  D G S TriJmos params:Device=1 Vto=-8 Kp=93m Mu=2.5
+ Ksubthres=0.5 Mtriode=0.3 VtoTc=-2.6m Bex=-1.5 m=1.3
+ Cgdmax=100p Cgdmin=90p a=1 Cgs=100p Rg=0.7 Msw=1
+ Isg=1f Ng=4 Egg=4.3 Rgs=5 v0=0 a0=3 v1=2 a1=2.7
+ v2=4 a2=2.2 v3=6 a3=1.6 v4=8 a4=1.3 v5=10 a5=1
+ v6=12 a6=0.9 v7=14 a7=0.8 v11=8 a11=1.3 v12=14 a12=1.3
+ v21=10 a21=0 v22=12 a22=2 v23=14 a23=5
.ENDS
```

3.3 2SK77 SIT

```
*TriJmos 1v5 (c) Ian Hegglun Dec 2019
.SUBCKT 2SK77  D  G  S
X1  D G S TriJmos params:Device=1 Vto=-2.5 Kp=0.38 Mu=3.8
```

```
+ Ksubthres=0.3 Mtriode=0.4 VtoTc=-10m Bex=-1.5 Msw=1 m=1.2
+ Cgdmax=8n Cgdmin=800p Cgs=3n Cjo=600p Rg=3
+ Isg=0.1p Ng=4 Egg=4.3 Rgs=3 mg=1 v0=0 a0=4 v1=1 a1=3
+ v2=2 a2=2.2 v3=3 a3=1.6 v4=4 a4=1 v5=5 a5=0.62 v6=6 a6=0.44
+ v7=7 a7=0.32 v8=8 a8=0.2 v9=9 a9=0.15 v10=10 a10=0.095
+ v11=4 a11=1.2 v12=6 a12=1.4 v13=8 a13=1.6 v21=4 a21=0 v22=5 a22=2
+ v23=6 a23=10 v24=7 a24=18 v25=8 a25=30 v26=9 a26=43 v27=10 a27=60
.ENDS
```

3.4 2SK82 SIT

```
*TriJmos 1v5 (c) Ian Hegglun Dec 2019
.SUBCKT 2SK82  D  G  S
X1  D G S TriJmos params:Device=1 Vto=-6.7 Kp=0.25 Mu=5
+ Ksubthres=0.3 Mtriode=0.4 m=1.4 VtoTc=-2.6m Bex=-1.5 Msw=1
+ Cgdmax=100p Cgdmin=90p Cgs=100p Rg=0.7 Isg=3f Ng=4 Egg=4.3 Rgs=4
+ v0=-1 a0=1 v1=0 a1=1.15 v2=2 a2=1.1 v3=4 a3=1.05 v4=6 a4=1 v5=8 a5=0.95
+ v6=10 a6=0.88 v7=12 a7=0.8 v8=14 a8=0.75 v9=16 a9=0.6 v10=18 a10=0.4
+ v11=6 a11=1.4 v12=18 a12=1.2 v21=4 a21=0 v22=6 a22=0 v23=8 a23=0
+ v24 =10 a24=0 v25=12 a25=3 v26=14 a26=10 v27=16 a27=16 v28=18 a28=20
.ENDS
```

3.5 2SK180 SIT j-FET (no plots available so scale 2SK182 Kp,C's by 0.33)

```
*TriJmos 1v5 (c) Ian Hegglun Dec 2019
.SUBCKT 2SK180  D  G  S
X1  D G S TriJmos params:Device=1 Vto=-1.1 Kp=2.5 Mu=4.5 m=1.5
+ Ksubthres=0.3 Mtriode=0.5 Bex=-1.5 VtoTc=-10m Msw=1
+ Cgdmax=3n Cgdmin=300p a=1 Cgs=2n Cjo=600p Rg=3 Isg=0.1p Ng=4 Egg=4.3 Rgs=3
+ v0=-1 a0=1 v1=0 a1=1 v2=1 a2=1 v3=3 a3=0.85 v4=5 a4=0.08 v5=10 a5=0.04
+ v6=15 a6=0.013 v7=20 a7=0.009 v8=25 a8=0.006 v9=30 a9=0.005 v11=0 a11=1.5
+ v21=0 a21=0 v22=1 a22=0 v23=3 a23=0 v24 =5 a24=9 v25=10 a25=40.5
+ v26=15 a26=108 v27=20 a27=203 v28=25 a28=301 v29=30 a29=410
.ENDS
```

3.6 2SK182 SIT j-FET

```
*TriJmos 1v5 (c) Ian Hegglun Dec 2019
.SUBCKT 2SK182  D  G  S
X1  D G S TriJmos params:Device=1 Vto=-1.1 Kp=7.5 Mu=4.5 m=1.5
+ Ksubthres=0.3 Mtriode=0.5 Bex=-1.5 VtoTc=-10m Msw=1
+ Cgdmax=12n Cgdmin=500p a=1 Cgs=7n Cjo=2n Rg=1 Isg=0.3p Ng=4 Egg=1.5 Rgs=1
+ v0=-1 a0=1 v1=0 a1=1 v2=1 a2=1 v3=3 a3=0.85 v4=5 a4=0.08 v5=10 a5=0.04
+ v6=15 a6=0.013 v7=20 a7=0.009 v8=25 a8=0.006 v9=30 a9=0.005 v11=0 a11=1.5
+ v21=0 a21=0 v22=1 a22=0 v23=3 a23=0 v24 =5 a24=9 v25=10 a25=40.5
+ v26=15 a26=108 v27=20 a27=203 v28=25 a28=301 v29=30 a29=410
.ENDS
```

3.7 Pass SIT1

```
*TriJmos 1v5 (c) Ian Hegglun Dec 2019
.SUBCKT SIT1  D  G  S
X1  D G S TriJmos params:Device=1 Vto=-4.1 Kp=3.8 m=1.45 Mu=15.5
+ Ksubthres=0.1 Mtriode=0.1 VtoTc=-2.6m Bex=-1.5 Trd1=20m  Msw=1
+ Cgdmax=800p Cgdmin=300p a=1 Cgs=670p Cjo=100p Rg=8
+ Isg=0.1p Ng=4 Egg=4.3 Rgs=1 ;gate diode
.ENDS
```

3.8 spare

The generic TriJmos subcircuit listing is provided in section Appendix 7
For updates check my SPICE model page

Appendix 4: TriJmos Parameter fitting steps for SITs

Fitting parameters is best done by starting with a Id vs Vgs plot using my jig (see Appendix 10). If you have a datasheet or bench measurements then set the jigs Vg range concentrate on the threshold region. Set Vds to the datasheet value.

Tip: If you have an existing jFET model then glean some of their parameters. But care is needed when converting threshold voltages from the jFET p/n format to the VDMOS format. The following conversions can be used to convert from the p/n jFET format:

```
Vto=VTO kp=2*BETA Rks=RS Rad=RD Isd=IS
+ Cgdmin=CGD Cgs=CGS Bex=BETATC -1 Vtotc=VTOTC
```

1. For SITs Rks and Rad can be initially set to a negligible value (set to 1u).

2. Set m=1.5 since SITs are usually a 3/2 power law. This sets the *low Vg* Mu – the Vg where they start to curve upwards (concave).

3. Generally Vto lies somewhere between the Vg's changing from *convex to concave*.

4. An approximate value for Kp is the change in drain current between two Vg steps (vertical difference). E.g. Vg is stepped 1V and the current changes by 2A then set Kp=2/1=2.

5. An approximate Mu value is the change in Vds/Vgs between steps. If Vg is stepped 1V and the Vds change is 10V then set Mu=10/1=10 as a start value. If the spacings are changing on the x-axis of the Id vs Vds plots then get the Mu value from gate voltages either side of the Vto, as above, where plots change from *convex to concave*.

6. For Mtriode plot the Id vs Vds curves with Vg steps as per the datasheet. For SITs Mtriode is likely to be fairly small in the 0.2 to 0.5 range. Mtriode changes the initial slope of the positive Vg plots and the rounding as current increases.

7. For Ksubthres parameter initially set it to 0.1. It determines the amount of rounding at very low currents ("knee" rounding).

8. If the Id vs Vds curves slope reduces as the Vg is more negative then you need to use the table parameters (v0,a0) through (v9,a9) and (v10,a10). To make choosing values easy use as many pairs as there are plots available (up to 11), or if time is limited use a pair for every second plot. The 'v' is the gate voltage and the 'a' is the relative slope. You assign a slope of 1 to the Vg closest to Vto that has some curvature (the one where the Mu and the power law 'm' is found above) – this is the reference curve that you fit first by changing Kp, Mu and Vto and lastly trim the power-law 'm'. Once this reference curve is fitted then the table is used to scale down the slope of each more negative curve one at a time with 'a'<1. Then more positive curves are scaled up one at a time with 'a'>1. If the curvature of the curves remains about the same and the Mu remains about the same, then you are about done. But if not, if the curvature changes with Vg and/or the Mu changes with Vg then you need to use another table (below).

9. The table for power-law changing with Vg uses points (v11,a11) through (v19,a19). Another table for Mu changing with Va uses points (v21,a21) through (v29,a29). Power-law changes with Vg are not very large (eg 1.5±0.3) and can use only 3 or 4 pairs. Mu changes can cover a very wide range in some SIT's, eg 2SK60, 2SK77, 2SK82, and 2SK182 and it is easiest to use one pair per Vg plot. Choosing the Mu shift as Vg gets more negative is easy since you enter the Vds offset into the 'a' value, where the offset is the Vds from the datasheet and the Vds with the fixed Mu. For example the 2SK182 from Vg=0V to Vg=-5V the curve shifts by about 20 volts on the x-axis. This gives a Mu of about 4.5. Then for a large negative Vg's like -30V the fixed Mu gives 140V but the datasheet shows 550V. So there is a 410V difference so we enter '410V' into table for the 30,410 pair. Enter all the other offset voltages and tweak the slope pairs (v0,a0) through (v9,a9) and (v10,a10) and you almost have it. Trim the power-law points. NB: If you find you need to change the Kp, Vto, Mu parameters then you will have to trim all the table parameters – this means you want to get the *reference plot* for Kp, Vto, Mu parameters as good as possible *before* doing any table parameters.

10. Next is temperature coefficients, mainly for Vto and Kp. If you have a Id vs Vgs datasheet plot with stepped temperatures then change VtoTc and Bex to get a similar crossing point, the zero temp co point (ZTC). Bex is negative in the range of -1 to -2.5 (default is -1.5). VtoTc is negative for n-channel and positive for p-channel (unlike standard SPICE jFETs!).

11 Choose capacitance values for Cgs, Cgdmin and Cgdmax where Cgs=Ciss and 10.

Cgdmin=Crss (both at higher Vds), Cgdmax≈2×Cgdmin or 3×Cgdmin seems OK for a jFET. (Cjo does not need to be defined since it is mostly from the body diode in the VDMOS which is disabled and by default the subcircuit sets Cjo to Cjo=Cgs to avoid raising the 'undefined parameter' error).

12. Choose gate diode values from a datasheet plot of Ig else use the I_{GSS} value (gate-source leakage). If no Ig data is available then use the default Is is the same as SPICE Is=1e-14 (10fA) which is in the ball-park for small and large jFETs. Alternatively find a similar jFET that has a datasheet with an Ig plot or I_{GSS} value. Plot log10(Ig) vs Vgs and change the Isg parameter (IS in jFETs) to get Ig passing though the datasheet value at the same Vgs. If you want to model drain-gate diode leakage current (I_{GSX}) then you need a Ig vs Vds plot – change the parameters Bvdl, Ibvl, Nbvdl, Rdl, kl, and set ml=1 (defaults are Bvdl=16, Ibvl=1p, Nbvdl=50, Rdl=100k, kl=10, ml=0). These give a changing amount of drain-gate diode leakage current (I_{GSX}) with drain-source voltage using a zener diode (Bvdl, Ibvl, Nbvdl) with a high value series resistance (Rdl) and a voltage amplification factor (kl) to set the Id offset with Vgs changes. Plot Ig vs Vds to see if the default values are satisfactory and tweak them if needed.

13. Noise parameters can be checked by plotting "V(onoise)" as described above.

We're about done. You can add the model to your library – see the section "How to use the above Model parameters" (covered above). It's now ready to use it in your amplifier.

Appendix 5: TriJmos Parameter listings for Triodes

5.1 12AT7

```
*TriJmosSqLin 1v5 (c) Ian Hegglun Dec 2019
.SUBCKT 12AT7  A  G  K
X1  A G K TriJmos params:Device=0 Vto=-0.35 Kp=1.58m Mu=30 m=1.5 Msw=1
+ Ksubthres=0.2 Mtriode=0.15 Cgs=2.3p Cgdmax=1.6p Cjo=0.4p VtoTc=0 Bex=0
+ Isg=100u Ng=4 Rgm=250 Rgs=82 kRg=0.5 Mug=1m mg=1
+ v0=-3 a0=2.4 v1=-2 a1=2.2 v2=-1 a2=1.9 v3=0 a3=1.35 v4 =0.5 a4=1 v5=1 a5=0.75
+ v6=2 a6=0.51 v7=4 a7=0.28 v8=6 a8=0.18 v9=8 a9=0.13 v10=10 a10=0.095
+ v11=-2 a11=1.1 v12=-1 a12=1.15 v13=0 a13=1.25 v14=0.5 a14=1.42
+ v15=1 a15=1.57 v16=2 a16=1.74 v17=4 a17=1.98 v18=6 a18=2.1
.ENDS 12AT7
```

5.2 12AU7

```
*TriJmos 1v5 (c) Ian Hegglun Dec 2019
.SUBCKT 12AU7  A  G  K
X1  A G K TriJmos params:Device=0 Vto=-0.3 Kp=0.53m Mu=12 m=1.5 Msw=1
+ Ksubthres=0.5 Mtriode=0.2 Cgdmax=1.6p Cgs=1.6p Cjo=0.33p VtoTc=0 Bex=0
+ Isg=40u Ng=4.2 Rgm=500 Rgs=200 kRg=0.1 mg=1
+ v0=-2 a0=1.8 v1=-1 a1=1.6 v2=0 a2=1.55 v3=2 a3=1 v4=4 a4=0.74 v5=8 a5=0.37
+ v6=12 a6=0.30 v7=16 a7=0.24 v8=20 a8=0.21
+ v11=-1 a11=1.35 v12=0 a12=1.35 v13=2 a13=1.5 v14=4 a14=1.6 v15=8 a15=1.9
.ENDS 12AU7
```

5.3 12AX7

```
*TriJmos 1v5 (c) Ian Hegglun Dec 2019
.SUBCKT 12AX7  A  G  K
X1  A G K TriJmos params:Device=0 Vto=-0.44 Kp=1.3m Mu=82 m=1.4 Msw=1
+ Ksubthres=0.3 Mtriode=20m Cgdmax=1.6p Cgs=1.6p Cjo=0.33p VtoTc=0 Bex=0
+ v0=-1 a0=1.3 v1=0 a1=1.11 v2=1 a2=1 v3=2 a3=0.91 v4=3 a4=0.73 v5=4 a5=0.6
+ v11=0 a11=1.27 v12=1 a12=1.4 v13=2 a13=1.7
+ Isg=40u Ng=4.2 Rgm=500 Rgs=200 kRg=1 Mug=1m mg=1
.ENDS 12AX7
```

The generic TriJmos subcircuit listing is provided in section Appendix 7

For updates check my SPICE model page

Appendix 6: TriJmos Parameter fitting steps for Triodes

Fitting parameters is best done by first setting Rad (internal anode/drain resistance) since this affects Kp. Set Rad and Rks to a small value (1u). Set m initially to 1.5.

1. For an initial guess for Kp set it to the gm of the tube *at 1/5th of the maximum anode current*, eg for the 12AX7 with a typical gm of 1.5mA/V at 1mA anode current set Kp to 1.5mA/V^$^{1.5}$. Then set Vto=0 initially.

2. Generally Vto lies somewhere between the Vg's changing from convex to concave.

3. For Ksubthres parameter initially set it to 0.1. It determines the amount of rounding at very low currents ("knee" rounding).

4. An approximate Mu value is the change in Vds/Vgs between steps. If Vg is stepped 1V and the Vak change is 10V then set Mu=10/1=10 as a start value. If the spacings are changing on the x-axis of the Id vs Vak plots then get the Mu value from gate voltages either side of the Vto where plots change from convex to concave.

5. For Mtriode plot the Id vs Vak curves with Vg steps as per the datasheet. For triodes Mtriode is likely to be fairly small in the 0.3 to 0.03 range. Mtriode changes the initial slope of the positive Vg plots and the rounding as current increases.

6. If the Id vs Vak curves slope reduces as the Vg is more negative then you need to use the table parameters (v0,a0) through (v9,a9) and (v10,a10). To make choosing values easy use as many pairs as there are plots available (up to 11 [footnote [13]]), or if time is limited use a pair for every second plot. The 'v' is the gate voltage and the 'a' is the *relative* slope; you assign a slope of 1 to the Vg closest to Vto that has some curvature (the one where the Mu and the power law 'm' is found above). This is the *reference curve* that you fit *first* by changing Kp, Mu and Vto and lastly trim the power-law 'm'.

7. Once this reference curve is fitted then the table is used to scale down the slope of each more negative curve one at a time with 'a'<1. Then more positive curves are scaled up one at a time with 'a'>1. If the curvature of the curves remains about the same and the Mu remains about the same, then you are about done. But if not, if the curvature changes with Vg and/or the Mu changes with Vg then you need to use another table (below).

8. The table for power-law changing with Vg uses points (v11,a11) through (v19,a19). Power-law changes were used for the 12AT7, 12AU7 and 12AX7. It seems the Island effect in these triodes changes the slopes as well as the curvature (power-law). But the power-law changes with Vg are not very large, like 1.5±0.3, and only 3 or 4 pairs may be are adequate.

9. Another table for Mu changing with Va uses points (v21,a21) through (v29,a29). Mu changes were needed for the 12AT7 but not the 12AU7 or 12AX7. For the 12AT7 it was easiest to use one pair per Vg plot. Choosing the Mu shift as Vg gets more negative is easy since you enter the Vak offset into the 'a' value, where the *offset* is the Vak from the datasheet and the Vak with the fixed Mu. Enter each offset voltages in the Mu table and tweak the slope pairs (v0,a0) through (v9,a9) and (v10,a10) and you almost have it. The power-law changes with Vg table points need tweaking. BTW If you find you need to change the Kp, Vto, Mu parameters then you will have to retrim all the table parameters – this means you want to get the *reference plot* right for Kp, Vto, Mu parameters *before* doing any table parameters.

---------- ----------

Appendix 7. TriJmos Generic subcircuit listing

The following generic subcircuit is for either a triode or jFET, where Device=1 for jFET and Device=0 for a Triode is set in each model instance.

13 You can use <u>any number</u> of pairs up to 11 for this table for slope but always start from v0,a0. The other power-law and Mu tables use (v11,a11) through (v19,a19) and (v21,a21) through (v29,a29) respectively (up to 9 parameters).

```
*TriJmos 1v5 (c) Ian Hegglun Nov 2019. *For jFET Device=1, for Triode Device=0
.SUBCKT TriJmos_  AD G KS ; Anode/Drain  Gate  Kathode/Source
*TriJmos 1v5 (c) Ian Hegglun Dec 2019
*For jFET Device=1, for Triode Device=0
.SUBCKT TriJmos  AD G KS ; Anode/Drain  Gate  Kathode/Source
R1 ksi KS {Rks*(1+Trs1*(Temp-25))}
M1 Di Gi ksi ksi vFET m={k}
B1 adi ksi I=Npwr(-I(H1),I(V2))*I(B3)
D1 N003 N005 Dg m={mg}
R6 AD adi {Rad*(1+Trd1*(Temp-25))}
I1 N003 N005 {Isg*T*U(mg)}
R3 G ksi {Rgleak}
D2 G Di Dd m={md}
E3 N002 ksi P001 ksi {-kl}
Vg1 P001 G {-Vto-VtoTc*(Temp-25)}
D4 N002 Di Dl m={ml}
B2 N007 ksi I=Tvak(V(adi,ksi),J,Ng)
R9 ksi 0 1e12
V1 ksi N007 {0}
H1 Di ksi V1 {1}
R7 N005 ksi R=1/(1/(Rgs*(1+kRg*V(Di,ksi)))+1/Rgm)
E1 N004 G Di ksi {Msw/Mu}
B6 G N003 V=T*Vto+Mug*Sqrt(V(Di,ksi))
M2 Di Gi ksi ksi vFETq m={1-k+1f}
B3 0 0 I=Table(-V(g,ksi),v0,a0,v1,a1,v2,a2,v3,a3,v4,a4,v5,a5,v6,a6,v7,a7,v8,a8,v9,a9,v10,a10)
;Island
V2 N006 ksi {0}
XX1 G G N006 ksi Table1 params:v1={v11} a1={a11} v2={v12} a2={a12} v3={v13} a3={a13} v4={v14}
+ a4={a14} v5={v15} a5={a15} v6={v16} a6={a16} v7={v17} a7={a17} v8={v18} a8={a18} v9={v19}
a9={a19}
XX2 G G N001 ksi Table1 params:v1={v21} a1={a21} v2={v22} a2={a22} v3={v23} a3={a23} v4={v24}
+  a4={a24} v5={v25} a5={a25} v6={v26} a6={a26} v7={v27} a7={a27} v8={v28} a8={a28} v9={v29}
a9={a29}
V3 N001 ksi {0}
H2 N004 Gi V3 {Msw/Mu} ;Vg(Va)
.model Dg D(IS={Isg} N={Ng} Eg={Egg} Rs={Rgs} Tnom=Temp)
.model Dd D(IS={Isd} N={Nd} Eg={Egd})
.model Dl D(IS={Isd} N={Nd} Eg={Egd} Rs={Rdl} Bv={Bvdl} Ibv={Ibvl} Nbv={Nbvdl})
.model vFET VDMOS (Vto={Vto+(VtoTc+1m)*(Temp-25)} Lambda={Lambda}
+ Rs=0 Rd=0 Rg=0 Mtriode={Mtriode} Kp={Kp*((Temp+273)/298)**(Bex+1.5)}
+ Ksubthres={Ksubthres*(1+Tksubthres1*(Temp-25))} Rds={Rds} Theta={Theta}
+ Cgdmax={Cgdmax} Cgdmin={Cgdmin} a={a} Cgs={Cgs} Cjo={Cjo} KF={Kf} AF={Af}
+ m={Mb} IS={Isb} N={Nb} Eg={Egb} Rb={Rb*(1+Trb1*(Temp-25))} ) ;Bv={Bv} Ibv=1m Nbv={Nbv}
.model vFETq VDMOS (Vto={Vto+(VtoTc+1m)*(Temp-25)} Lambda={Lambda}
+ Rs=0 Rd=0 Rg=0 Mtriode={kt*Mtriode} Kp={Kp*((Temp+273)/298)**(Bex+1.5)}
+ Ksubthres={Ksubthres*(1+Tksubthres1*(Temp-25))} Rds={Rds} Theta={Theta}
+ Cgdmax={Cgdmax} Cgdmin={Cgdmin} a={a} Cgs={Cgs} Cjo={Cjo} KF={Kf} AF={Af}
+ m={Mb} IS={Isb} N={Nb} Eg={Egb} Rb={Rb*(1+Trb1*(Temp-25))} ) ;Bv={Bv} Ibv=1m Nbv={Nbv}
.function Tvak(Vak,J,Na) {If(J,Vak,Na*26m*Le(Vak/(Na*26m)) )}
.function Npwr(Iin,p) {If(U(Abs(p-2)),Kp/m*(m/p)**p*Pwrs(Iin*2/Kp,p/2), Iin)}
.function Le(X) { If(U(X-450), X, Ln(1+Exp(X))) } ;Unlimited Ln(1+e^X)
.param device=1  J=U(device) T=Inv(J)  ;1=J(FET),0=T(riode)
+ Vto=0 Kp=1 k=1 Ksubthres=0.1 Mtriode=1 kt=0 Lambda=0 m=2 Mu=10 Msw=0 ;Mu disaled for jFET
+ Rks=1u Rad=1u Rds=1G VtoTc=-1m Bex=-1.5 Tksubthres1=0 Trs1=0 Trd1=0m KF=0 AF=1 Bv=1G Nbv=1
+ Cgdmax=0p Cgdmin=Cgdmax a=1 Cgs=0p Cjo=Cgs Rg=0 Theta=0 Rgleak=1e12
+ Mb=0.5 Isb=1e-14 Nb=1 Egb=1.11 Rb=1e12 Trb1=0 ;body diode=disabled
+ Isg=1e-14 Ng=1 Na=1 Egg=1.11 Rgs=1u Rgm=2*Rgs kRg=0 Mug=0 mg=1 ;jFET g-s diode=enabled
+ Isd=Isg Nd=Ng Egd=Egg md=J ;main g-d diode=enabled if JFET
+ Bvdl=16 Ibvl=1p Nbvdl=50 Rdl=100k kl=10 ml=0 ;g-d leak diode=disabled
+ v0=0 a0=1 v1={v0} a1={a0} v2={v1} a2={a1} v3={v2} a3={a2} v4={v3} a4={a3} v5={v4} a5={a4}
+ v6={v5} a6={a5} v7={v6} a7={a6} v8={v7} a8={a7} v9={v8} a9={a8} v10={v9+1} a10={a9} ;Island
+ v11=0 a11={m} v12={v11+1} a12={a11} v13={v12} a13={a12} v14={v13} a14={a13} v15={v14} a15={a14}
+ v16={v15} a16={a15} v17={v16} a17={a16} v18={v17} a18={a17} v19={v18} a19={a18} ;pwr-law
+ v21=0 a21=0 v22={v21+1} a22={a21} v23={v22} a23={a22} v24={v23} a24={a23} v25={v24} a25={a24}
+ v26={v25} a26={a25} v27={v26} a27={a26} v28={v27} a28={a27} v29={v28} a29={a28} ;Vg(Va)
.ENDS TriJmos

.Subckt Table1 X In Y ref
R1 X 0 1e12
R2 In 0 1e12
R4 Y 0 1e12
R3 ref 0 1e12
```

```
B1 ref Y I=(Table(-V(x,ref),v1,a1,v2,a2,v3,a3,v4,a4,v5,a5,v6,a6,v7,a7,v8,a8,v9,a9) -0)
.param v1=0 a1=1 v2={v1} a2={a1} v3={v2} a3={a2} v4={v3} a4={a3} v5={v4}
+ a5={a4} v6={v5} a6={a5} v7={v6} a7={a6} v8={v7} a8={a7} v9={v8} a9={a8}
.ENDS Table1
```

A demo circuit with all the above models can be download (see my Spice Models page). Appendix 9 explains how to use this jig.

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Appendix 8.
TriJmos jFET, SIT & Triodes – Summary Table of Parameters

[to be completed]

Params	SJEP120R100	2SK60	2SK77	2SK82	2SK180	2SK182	SIT-1	LSK389B	LSK489B	LSJ689B	BF545B	2SK170B	LSJ74B	2SK932-23	12AT7	12AU7	12AX7	Params
Vto	0.9							_	_	_	_	_	_	_	-0.35	-0.3	-0.44	Vto
Kp	24							70m	9m	8m	2.7m	70m	160m	150m	1.58m	0.53m	1.3m	Kp
Ksubth	0.1							_	_	_	_	_	_	_	0.2	0.5m	0.3	Ksubth
Lambda								2m	1m	0.6m	2m	2m	7m*	3m				Lambda
k								_	_	_	_	_	_	_				k
kt								_	_	_	_	_	_	_				kt
m	100														1.5	1.5	1.4	m
Mtriode	0.7														0.15	0.2	20m	Mtriode
Rks	14m																	Rks
Rad	45m																	Rad
Mu	100	2	5.2	2.15	5	5	15								30	12	82	Mu
Msw	1														1	1	1.3m	Msw
Isg	1f		_	_	_	_									0.1m	40u	40u	Isg
Ng			_	_	_	_									4	4.2	4.2	Rgs
Rgs	0.7														82	200	200	Rgm
Rgm															250	500	500	kRg
kRg															0.5	0.1	0.1	kRg
Mug															1m			Mug
KpTable															11	11	6	KpTable
mTable		_					_								9	9	3	mTable
MuTable		_					_											MuTable
OK?	√														√	√	√	OK?
# used	11	1	3	3	3	3	1	6	6	6	6	6	6	6	13	12	12	# used

---------- ----------

Appendix 9.
How to use TriJmos the demo jig

The finalised models are in '**PAK213-Appendix-TriJmos-jigs.zip**' on my Spice Models page). You can run any of my models using this file. Make sure all the associated files are in the same directory. To select a model change the part name for J3 to any of those provided. Set the Vg step range by commenting out the existing one and enable the required one. Set the "Vin" range (top right) to the value specified in the Vg step list. Run and view the current as I(R2).

The jig I used to extract and collect and plot all my models is also available; look for '**PAK213-Cct-TriJmoB-SIT-Triode-TUX.zip**'. This is a similar jig to above but only for Triodes and SIT's. It contains Table B-sources with captured data points from datasheets (the 12AT7 has measured points courtesy of Adrian Immler, thanks again Site here and data for 12AT7). Use this if you want to fit your own model triode; copy an existing one, rename it, set the Vg steps and Vin range, then follow the parameter fitting steps in Appendix 6. For model parameters using the tables change the Vg (v0,a0) to (v9,a9) values to suit your triode datasheet (any number of

pairs up to 11 pairs).

When you are happy with the plots,place your model in your amplifier. You place a n-FET and change the prefix to 'X' for a subcircuit, then add the model name. Copy the model listing to your circuit (press 'S' and paste). Then copy the main subcircuit text and the Table1 subcircuit. You can now run your new model. To avoid clutter place the models in a txt file and add .include <model-file>.txt on your schematic. When you use the TriJmos as a stand alone 'Cell' model you don't need any of the .asy files (they are for development purposes for the 'Block' version), just the <model-file>.txt needs to be with your circuit (.asc) file.

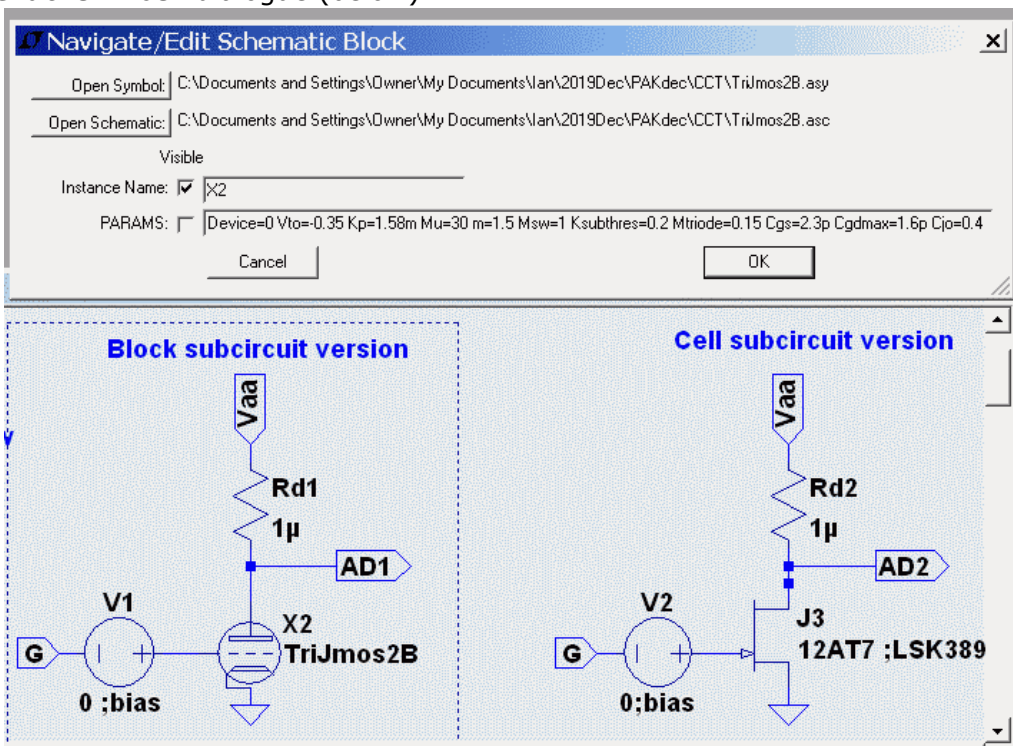
---------- ----------

Appendix 10.
How to embed TriJmos Block parameters using Attribute Editor

This is for embedding TriJmos parameters for 'Block' subcircuits using Attribute Editor. You only need to do this for development purposes if you want to modify the TriJmos code or want to create a subcircuit of your own using my model as an example to see how to do it.

I found 'Block' subcircuits need <u>every</u> step done <u>exactly</u> right otherwise they won't work! They can be frustrating. But once working you don't need to use a Netlist to develop and test a subcircuit. At the end of development you convert the Block to run as a Cell subcircuit for your use in your amp and for sharing with others (see the end of this section).

When you run the 'PAK213-Cct-TriJmos.asc' file you can Right-Clk on X2 to open the **`Navigate Edit Schematic Block`** dialogue (below).



'Block' parameters can be embedded into the attributes so it links to the Generic TriJmos subcircuit.

From here you can open the **`model.asy`** symbol or the **`model.asc`** circuit. But for this sessio we want to copy and paste a model parameter list into this instance (rather than take the parameters from **`.param x=...`** statements on the top page). Pasting the parameters in this way means you can have *several instances* of the same TriJmos Block circuit running all at the same time. To past the models into the **`params:`** area you can use a word processor to get all

the parameters into one string (maybe from an existing Cell model parameter listing by removing all the line returns). Once pasted into this are you can run the model.

If you Ctrl+RightClk on the component again you get the Attribute Editor showing all the Attributes. You can see the **`params:`** area (pasted above) end up in the SpiceLine area. But if you have pasted more than 250 characters into the **`params:`** area (SpiceLine) then you get a message saying we can't display more than 250 characters. Don't worry if you can't view them with the Attribute Editor because you can still view and edit them via the **`Navigate Edit Schematic Block`** dialogue using just Rt-Clk on the component. And if you do really need to get to the Attribute Editor you can Cut the **`params:`** area (to the Clipboard) to get to the Attribute Editor, view it, then when done paste the **`params:`** area back.

How to set up subcircuit attributes in LTspice (so they actually run)

If you are new to LTspice and subcircuits, to change a jFET symbol to accept a part that uses a subcircuit you need to change the "Prefix" flag from "JN" to either A) "X" (for a 'Cell' subcircuit), or B) nothing (for a 'Block' subcircuit).

To access the Component Attribute Editor use Ctrl+RtClk with the cursor on a new jFET symbol.

Enter the part name in the "SpiceModel" area – For a Cell this must be the same as the subcircuits name, eg in the line: `.SUBCKT` **`LSK389B`** `D G S` . But for a Block subcircuit this text does not call any subcircuit so you can use whatever you like (even **`LSK389B`** same as a Cell version).

Finally a 'Block' subcircuit (circuit) can be converted to text a netlist using View > SPICE Netlist and then Copy/Paste the main 'Cell' subcircuit text netlist (or into an old netlist to update it). Before the text code is the '**`.SUBCKT <model> X Y Z`**' (x,y,z pins). At the end of the text code is '**`.ENDS`**'.

Appendix 11. TriJmos parameter descriptions for jFETs, SITs & Triodes

The following are standard VDMOS parameters, used by TriJmos model with the same names

Name	Description	Units	Default	Example	Example	Example
	Inbuilt VDMOS params			**jFET**	**SIT**	**Triode**
Vto*	Threshold voltage*	V	0	-2	-3	-0.1
Kp	Transconductance parameter (Triode Vg=0)	A/V^2	1	10m	5	5m
Lambda	Channel-length modulation	1/V	0	2m	-	-
mtriode	Independent fit of triode and satn regions	-	1	0.5	0.5	0.2
Ksubthres	subthreshold conduction parameter	-	0.1	0.1	0.1	0.1
BV	Vds breakdown voltage	V	Infin.	40	-	-
IBV	Current at Vds=BV	A	100pA	1u	-	-
NBV	Vds breakdown emission coefficient	-	1	10	-	-
Rg	Gate ohmic resistance	Ω	0	10	1	-
Rds	Drain-source shunt resistance	Ω	Infin.	1G	1G	1G

Rb	Body diode ohmic resistance	Ω	0	1e12	1e12	1e12
Cjo	Zero-bias body diode junction capacitance	F	0	1n	1n	1p
Cgs	Gate-source capacitance	F	0	25p	600p	2p
Cgdmin	Minimum non-linear G-D capacitance	F	=Cgdmax	5p	40p	-
Cgdmax	Maximum non-linear G-D capacitance	F	0	20p	1n	1p
a	Non-linear Cgd param	-	1	-	-	-
Af	Flicker noise exponent	-	1	-	-	-
Kf	Flicker noise coeff.	-	0	-	-	-
Bex	Power of Kp temp depend	-	-1.5	-	-	0
Vtotc*	Vto tempco. If specified -1mV/°C based on phi is ignored*.	V/°C	-1m	-2m	-2m	0
Tksubthres1	linear tempco of Ksubthres	$°C^{-1}$	0	0	0	0
Trs1	Rs linear tempco	$°C^{-1}$	0	3m	3m	-
Trd1	Rd linear tempco	$°C^{-1}$	0	3m	3m	-

* Polarity of VDMOS Vto and Vtotc is reversed for p-channel. For the **TriJmos** p-channel **don't reverse** these polarities since the n-to-p subcircuit does it.

The following are additional parameters used by TriJmos model

Name	**Description**	**Units**	**Default**	**Example**	**Example**	**Example**
	Native TriJmos params			**jFET**	**SIT**	**Triode**
Device	Selects Triode or jFET	-	1	1	0	0
Rks	Cathode/Source resistance	Ω	1u	10	-	-
Rad	Anode/Drain	Ω	1u	8	1	100
Mb	Body diode M	-	0.5	-	-	-
Isb	Body diode Is	A	1E-14	-	-	-
Nb	Body diode N	-	1	-	-	-
Egb	Body diode Eg	eV	1.11	-	-	-
m	Power-law	-	2	2	1.5	1.5
Mu	Feedback factor at Vg=0	-	1k	-	15	40
Msw	Switch for Mu(Va) Msw =0 disables Mu(Va)	-	0	0	1	1
Isg	Grid/gate diode Is	A	1E-14	10f	100n	40u
Ng	Grid/gate diode N	-	1	-	-	4
Rgs	Grid/gate diode Rs	Ω	1u	-	-	100
Rgm	Grid Rs shunt R	Ω	2*Rgs	-	-	500
kRg	Grid Rs change with Vg	1/V	0	-	-	0.2
Mug	Grid diode Mu feedback	-	0	-	-	1m
mg	Grid/gate diode switch	-	1	1	1	1

Egg	Gate to Source diode Eg	eV	1.11	-	4	-
Rgleak	Grid to Kathode leak R	Ω	1e12	-	-	-
Na	N for Vak to Vds	-	1	-	-	-
Isd	Is for Gate-Drain diode	A	=Isg	-	-	-
Nd	N for Gate-Drain diode	-	=Ng	-	-	-
Edg	Eg for Gate-Drain diode	eV	=Egg	-	-	-
md	M for Gate-Drain diode	-	1	1	1	0
Bvdl	Bv for Gate-Drain zener	V	16	16	-	-
Ibvl	Ib for Gate-Drain zener	A	1p	1p	-	-
Nbvdl	N for Gate-Drain zener	-	50	50	-	-
Rdl	Rs for Gate-Drain zener	Ω	100k	100k	-	-
kl	Vds scaling for Gate-Drain zener	V/V	10	10	-	-
ml	M for Gate-Drain diode	-	0	1	0	0
v0,...,v10	Island Vg points	V	0	-	range	range
a0,...,a10	Island Kp scale factors	-	1	-	range	range
v11,...,v19	Power-law Vg points	V	0	-	range	range
a11,...,a19	Power-law values	-	=m	-	range	range
v21,...,v29	Table for Mu Vg points	V	V	-	range	range
a21,...,a29	Table for Mu ΔVa points	V	ΔV	-	range	range

Note 1: A **'-'** dash signifies **not applicable**, it doesn't matter what value is used because the default gets invoked.

*Note 2: There is no switch parameter for the TriJmos to select p-channel. Instead the TriJmos the p-channel uses a special subcircuit to reverse the n-channel currents and terminal polarities (see text).