# A simple pulse test jig

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A companion paper for: 'VDMOS Parameter Extraction with subthreshold conduction'

This pulse jig is kept as simple as possible while still providing accurate readings from power MOSFET's.

Two AC SSR's are used as Sample/Hold switches and work with either polarity p-channel or n-channel MOSFET's simply by reversing the batteries supplying the power MOSFET's. **Figure 1** shows the pulse jig circuit.

**Figure 2** shows the pulse generator and the Solid State Relay's (SSR's).

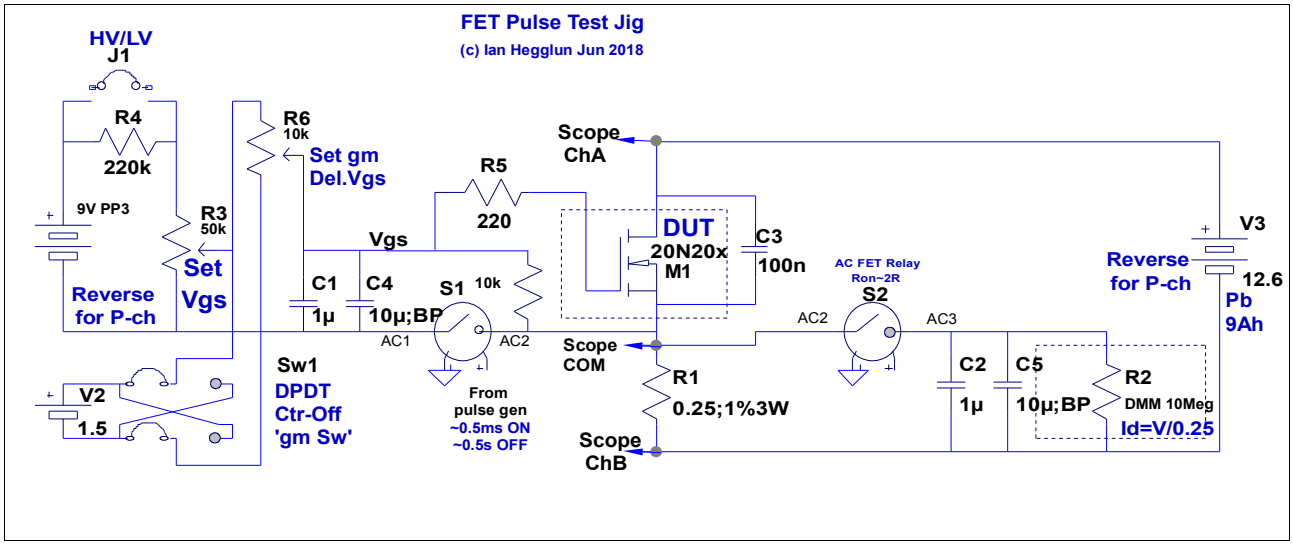


**Figure 1. Pulse test jig circuit**

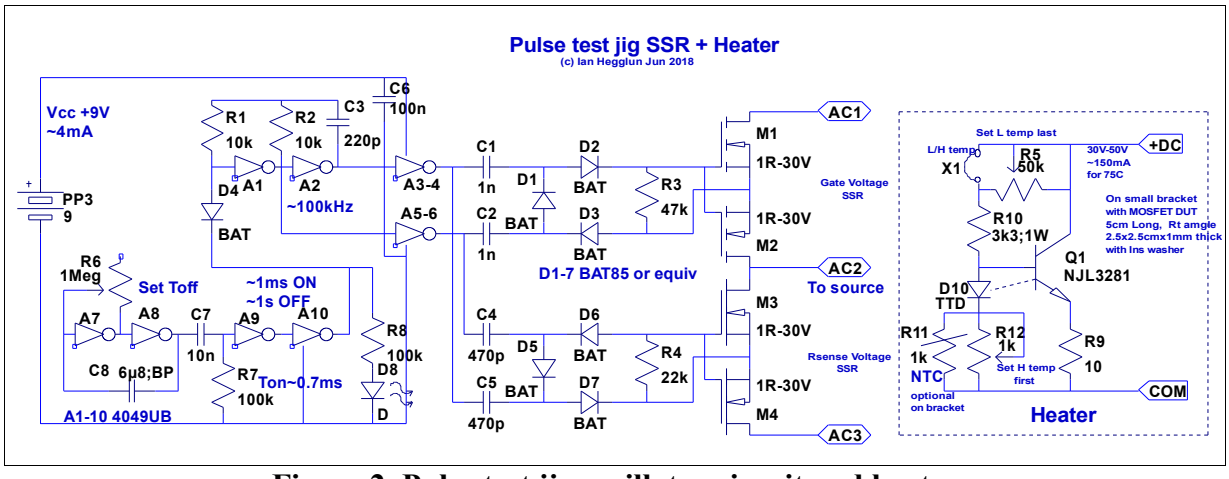


**Figure 2. Pulse test jig oscillator circuit and heater**

**Figure 3** shows the bench layout.

This test jig can measure high currents or high voltage devices. The current pulse and voltage levels depend only on the main battery size and the current sensing resistor, or the HV power supply for testing tubes. Pulse ON time can be between 300us and 1ms which is fast enough that thermal changes of the junction do not alter the Id during the ON period. A pulse ON time between 300µs and 1ms does not require a fast switching Sample and Hold allowing a simple circuit.

The pulse OFF period is between 0.5 second and 1 second, which is long enough between pulses to keep the average power dissipation low allowing a small heatsink and a rapid heatsink heater warm up and settling time. Also the time between pulses is not too long allowing meter readings settle to

less than 0.1% in a few seconds without needing an special opamp buffer.

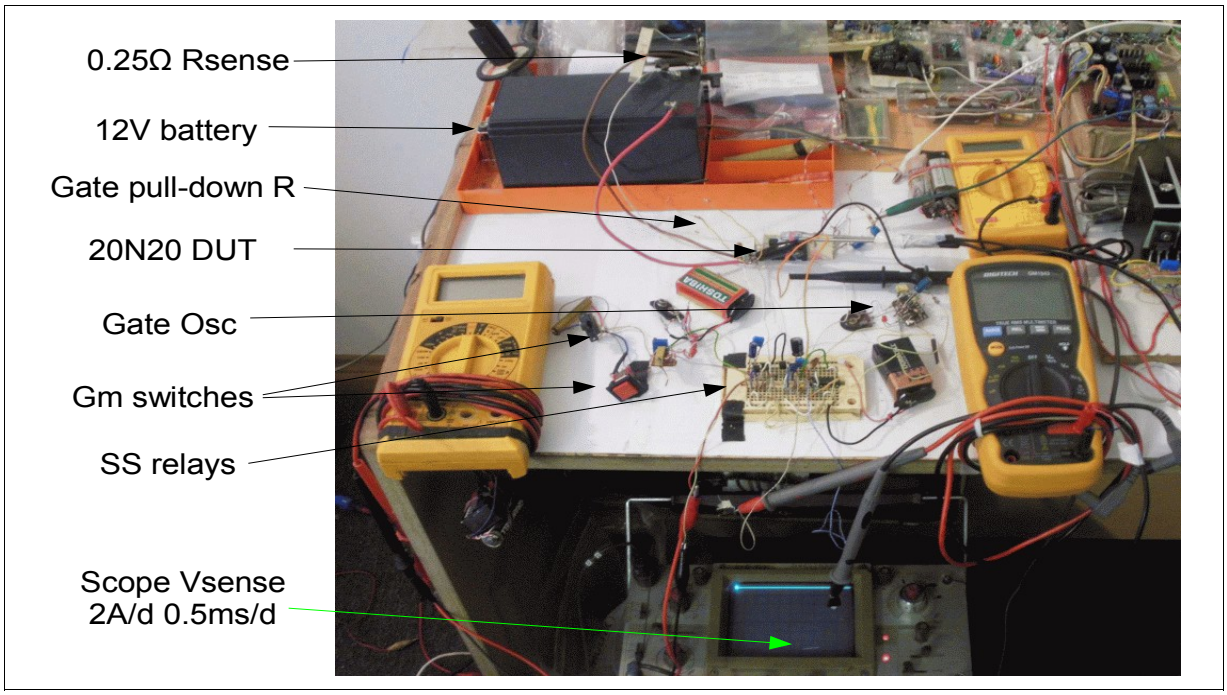


**Figure 3. Test jig. The scope shows droop in Id at 14A with 0.7ms pulse & 2Hz repeat**

The pulse jig applies a voltage to the gate of the MOSFET through an AC solid-state relay from a capacitor that is pre-charged to the test voltage. The capacitor is 10uF which is large enough to give an almost constant voltage across to the gate with a discharge resistor between gate and source. Since the gate Solid State Relay is SPST the gate has a discharge resistor to pull its voltage back to 0V. The charge time constant is around 10 microseconds using a SS relay with an ON resistance of a few ohms.

The MOSFET's ON state pulse current is measured as the voltage across a low ohm series resistor, where the voltage is transferred to a storage capacitor via another Solid State Relay. The storage capacitor feeds a 10 Meg input resistance DMM for a very long discharge time constant (10uF and a 10 Meg gives a 100 second time constant). During the ON time there is some droop in the drain current and this can be calibrated out by measuring the drain current for several ON times, eg 1.4ms, 0.7ms and 0.35ms were used. The variation in the 3 readings are plotted to find the value at the start of the ON time.

Plots were done for the 10N20 (10x20 are 10A devices) and the 20N20 (20A devices). See the spreadsheet (download). The sense resistor is 0.25 ohms for the 20A devices and 0.5 ohms for the 10A devices. The 10A devices are tested at 100mA, 1A and 4A to check the change in slope with current current. Typical *Slope Factor* was 1-2% at 1A to 4A. A fixed *Slope Factor* was applied to all the currents in the spreadsheet for parameter extraction. Scaled results for Id, gm and d(√Id) were then exporting to a csv file and pasted into LTspice as Table data for tweaking parameters.

With a sample time of 300us the drain current was measured to the accuracy of the sense resistor's tolerance of ±1% for my jig resistor.

My test jig allows accurate gm measurements by calculating the difference in drain current for a small gate voltage change (±50mV). Gm requires the difference of two currents with a small difference in gate voltage. Normally gm measurement contain a lot of measurement 'noise' but this jig keeps the noise to within a few percent, allowing nice and smooth gm plots, which is the key to simpler and more accurate parameter extractions.

Measurements were done in 100mV steps up to about 1A for a 20N20 and then 250mV steps to about 8A, and lastly 1V steps to 20A. After plotting in the spreadsheet, usually one or two points appear to be off the general trend; so checking the spreadsheet values often it is found that the

number was entered incorrectly into the spreadsheet, and less frequently a meter read or incorrect writing of a reading.

When changing from 10Ω sense resistor to 0.25Ω the readings were repeated at the same gate voltage and the calculated Id and gm values were compared and if they were more than 1% different then the 10R values were scaled to get the common points to match within 1% (by altering the 10Ω value for scaling Id, and altering the ΔVgs voltage used to calculate gm).

For the ALFET's the gate voltage change was ±50mV for currents up to 0.5A then ±100mV for all higher currents. The key to get accurate gm's is a ±Vgs *centre-off switch* to raise and lower Vgs by a consistent increment over a few seconds.

A 0.25 ohm sense resistor was used for the 20N20 and 20P20 (ALFET's) which allowed readings to 15A and down to 1mA still with a 100 step resolution using a 4.5 digit DMM. For subthreshold measurements down to 10uA the sensing resistor was changed to 10 ohm up to a few milliamps.

Since the heating with subthreshold current measurements is negligible the SSR's was bypassed (with wire links) and the clocking stopped to remove any feed though for measurement. Currents down 0.01uV across a 10 ohm sense resistor with a 4.5 digit DMM measured to 10uA with 2 digit resolution.

### *Plotting example: Exicon 10N20, 10P20, 20N20 and 20P20*

**Figure 4** shows the finalised VDMOS current Id(M3)(Cyan) 25C (higher Id's) and 75C (lower Id's). The measured values are Red. VDMOS includes parameter Mtriode for a better fit at Vds~5V.

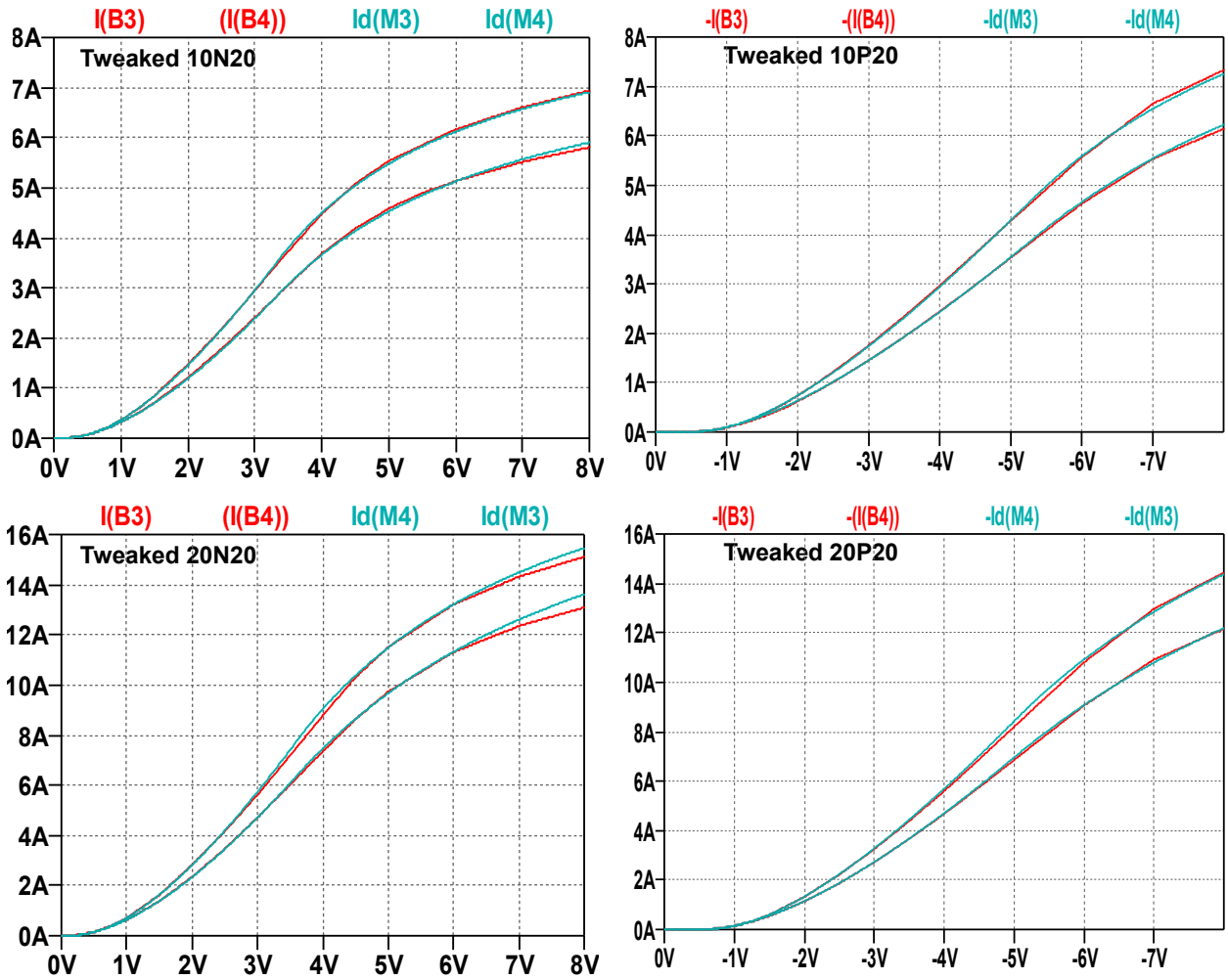


**Figure 4. Tweaked VDMOS Id (Cyan) and measured Id (Red)**
**Plots are 25C (higher Id's) and 75C (lower Id's)**

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